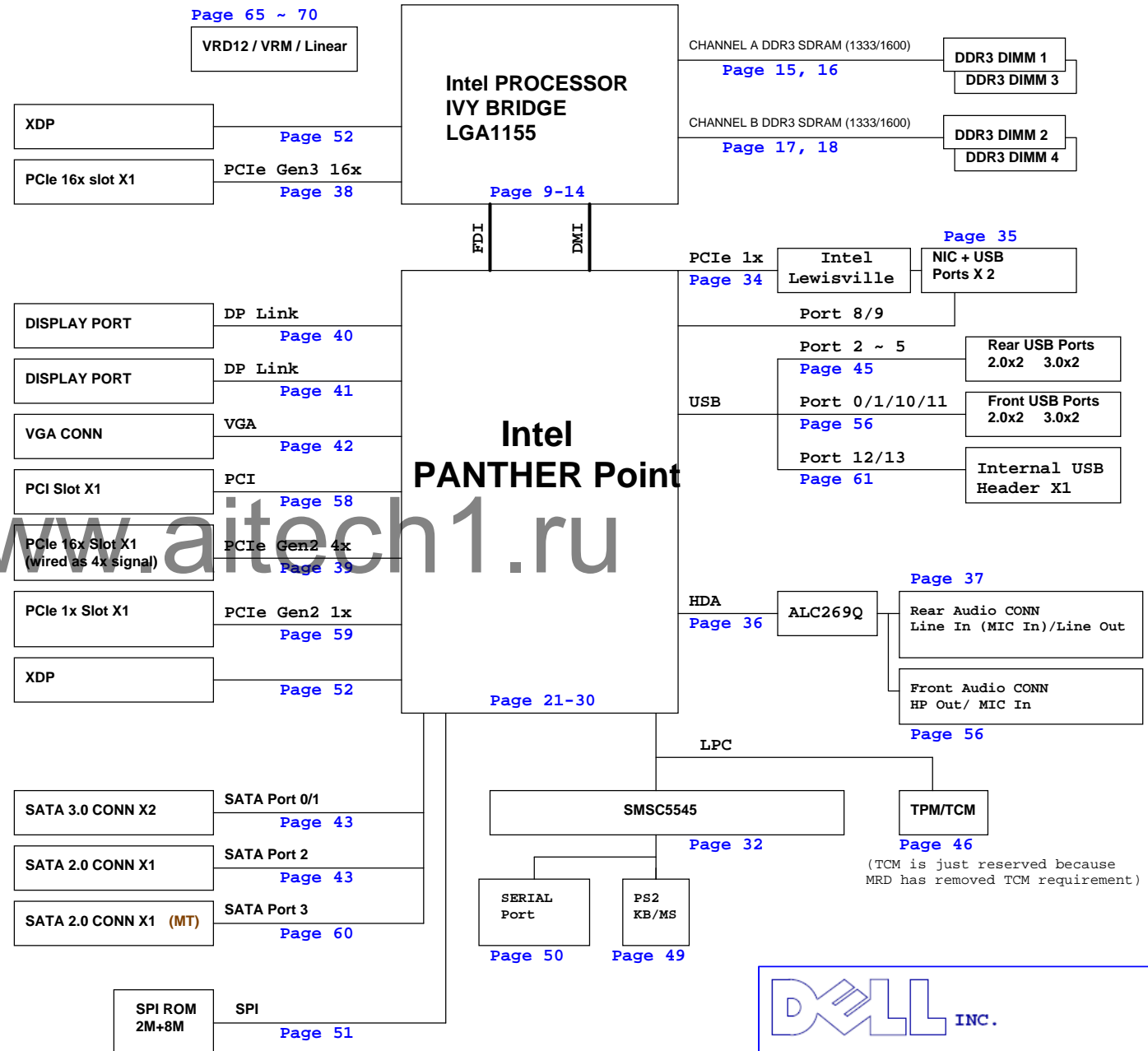


Lainikai - MT / DT

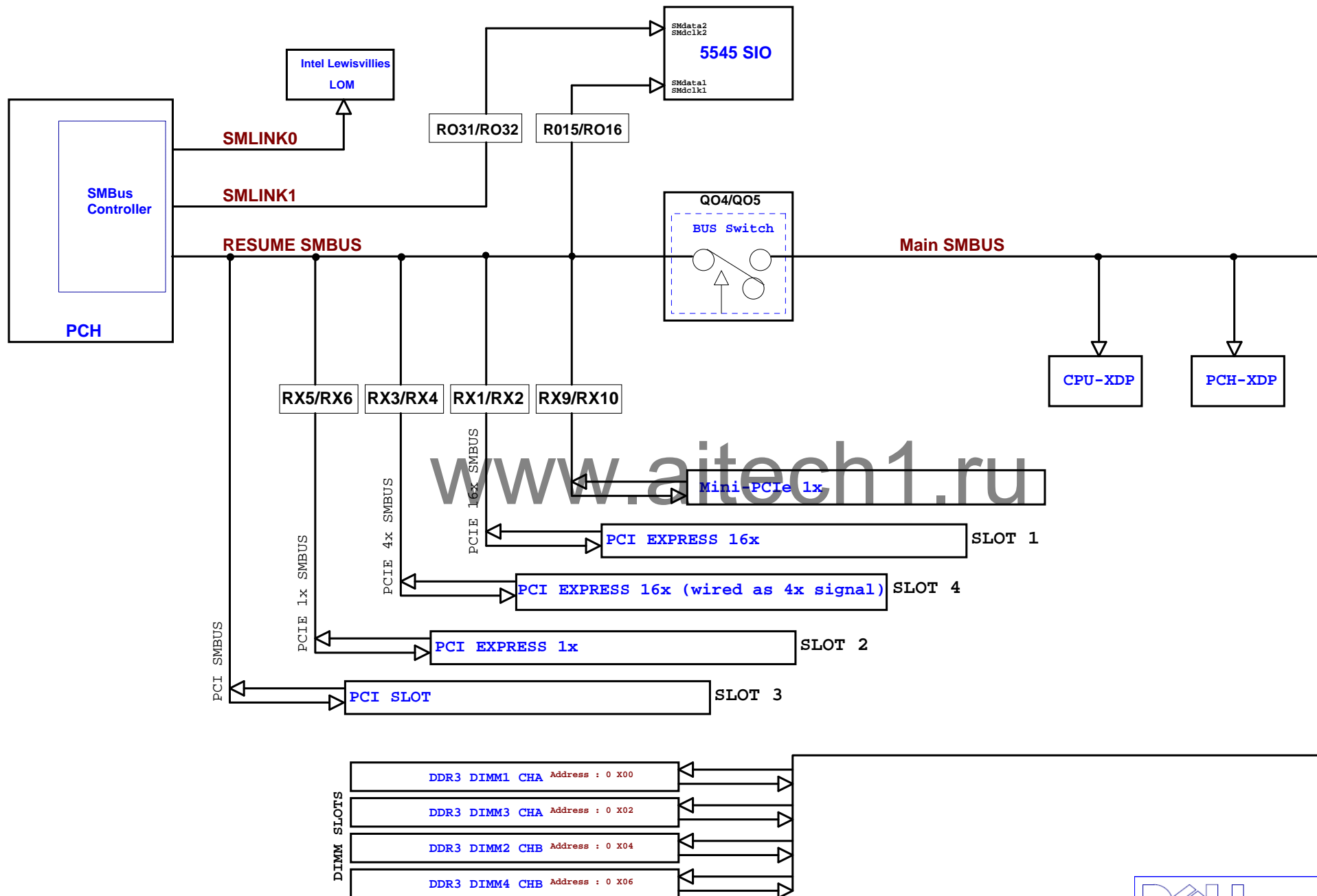
1. Index / Block diagram
2. SMBus MAP
3. Clock Distribution
4. Power Delivery Map
5. Power On Sequence
6. Reset / Power Good Map
7. Strap/IRQ/IDSel Table
8. GPIO Table
- 9-14. CPU
- 15-16. DDR3 Conn: CHA
- 17-18. DDR3 Conn: CHB
19. TBD
20. TBD
- 21-30. PCH
31. PCH MISC Conn/BUZ/ID
- 32-33. SIO:SMSC5544
- 34-35. LAN: INTEL LEWISVILLE
- 36-37 AUDIO:ALC269Q
38. Slot1: PCIe 16x
39. Slot4: PCIe 4x
40. Display Port 1
41. Display Port 2
42. VGA Conn
43. SATA Conn
44. TBD
45. Rear USB
46. TPM & TCM
47. Thermal Sensor Conn
48. FAN
49. PS2 Conn
50. COM1
51. SPI
52. XDP
53. Pilot Run Conn
54. EMI
55. COM2 HDR
56. Front Panel
57. Front USB 3.0
58. Slot3: PCI
59. Slot2: PCIe 1x
60. SATA_MT
61. Flexbay USB
62. TBD
63. Power Conn
64. Power Sequence
- 65-66. Power: Linear Power
- 67-68. Power: Vcore PWM
- 69-70. Power: VCCIO/VCCSA
71. Power: DDR3/5Vdual/5VUSB

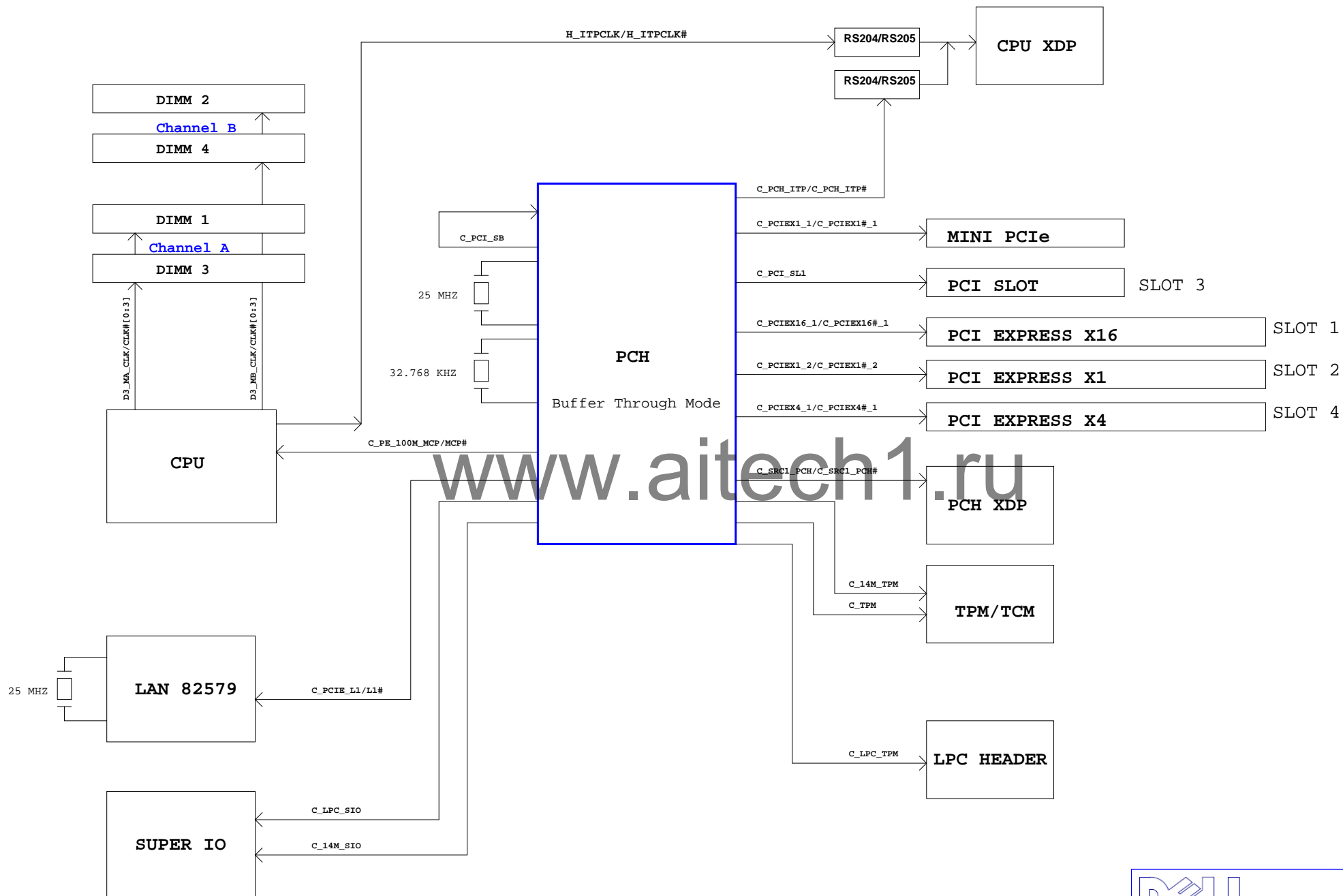


| DESIGN | CHECK | APPROVE |
|--------|-------|---------|
| Hiko | Hiko | Ivan |

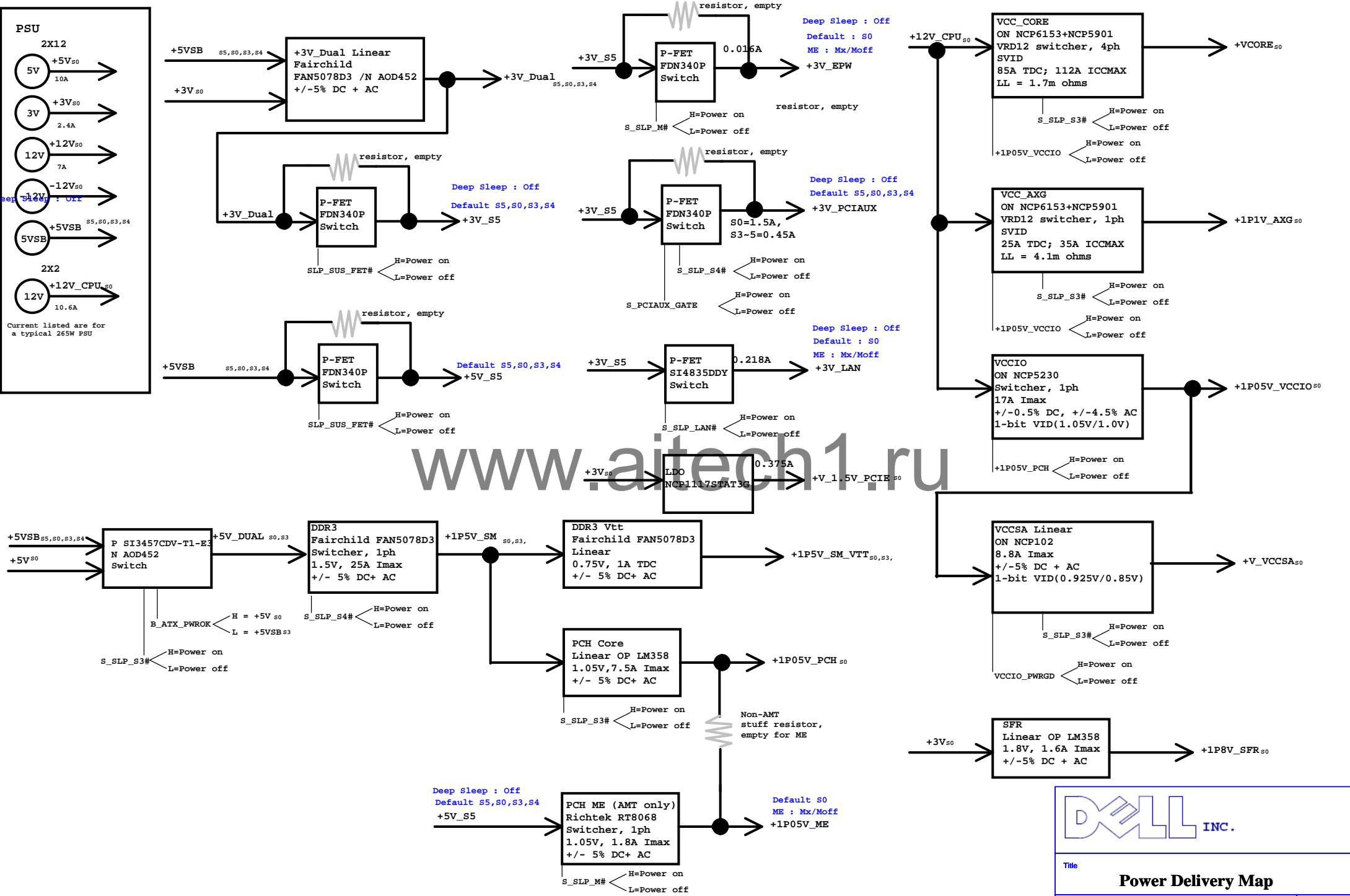
| | | |
|--------------------------------|---------------|---------|
| DELL INC. | | |
| Title | | |
| Index / Block diagram | | |
| DWG NO | Lanikai_MT/DT | Rev A00 |
| Date: Wednesday, June 13, 2012 | Sheet 1 | of 71 |

SMBUS DIAGRAM





POWER DELIVERY MAP



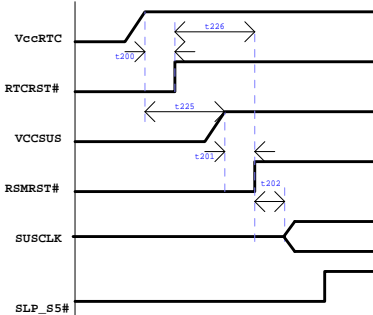
DELL INC.

Title: **Power Delivery Map**

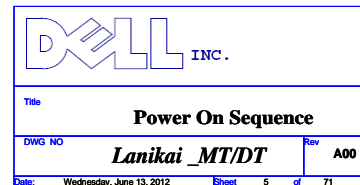
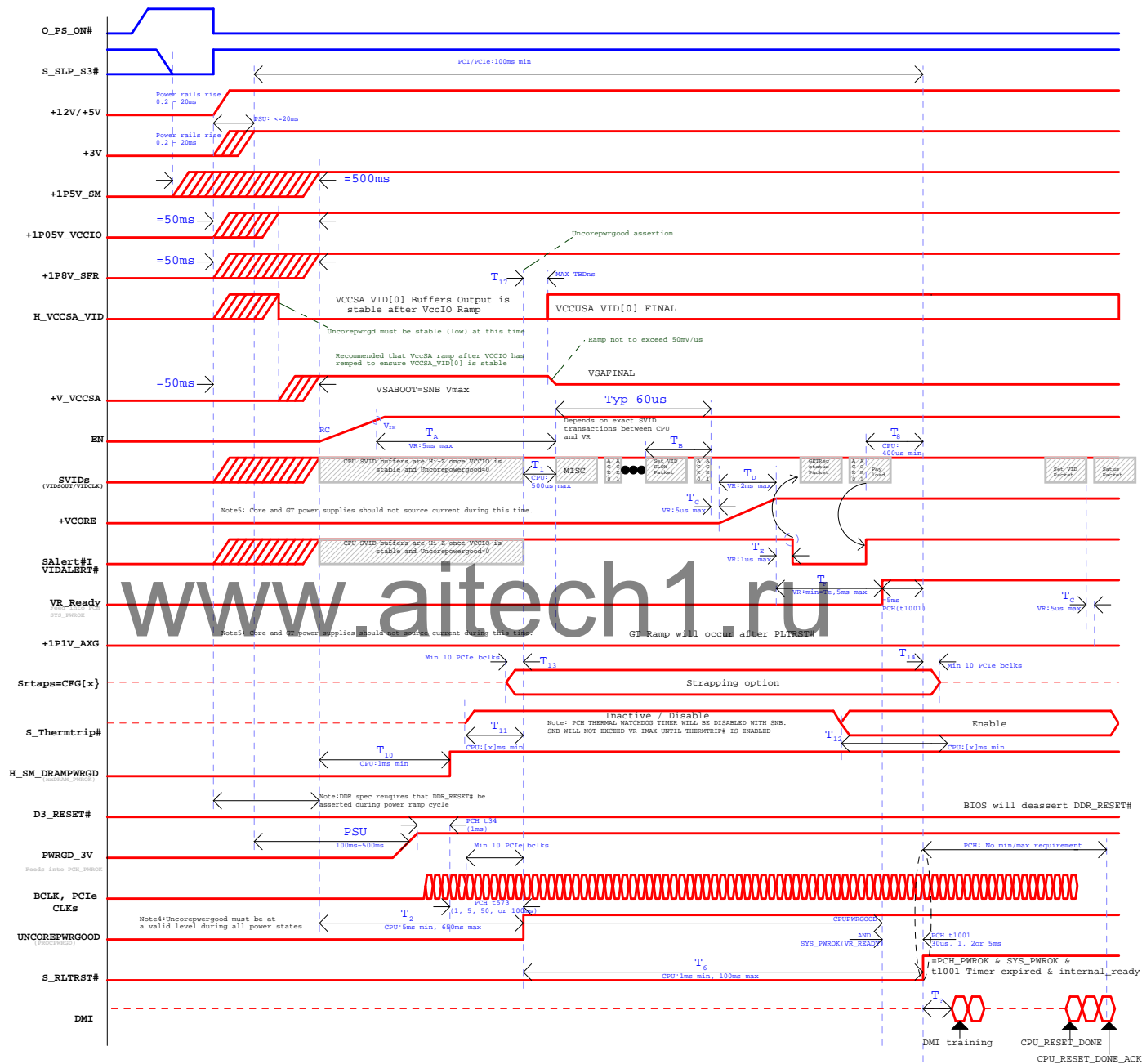
DWG NO: **Lanikai_MT/DT** Rev: **A00**

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G3 to S4/S5 Timing Diagram



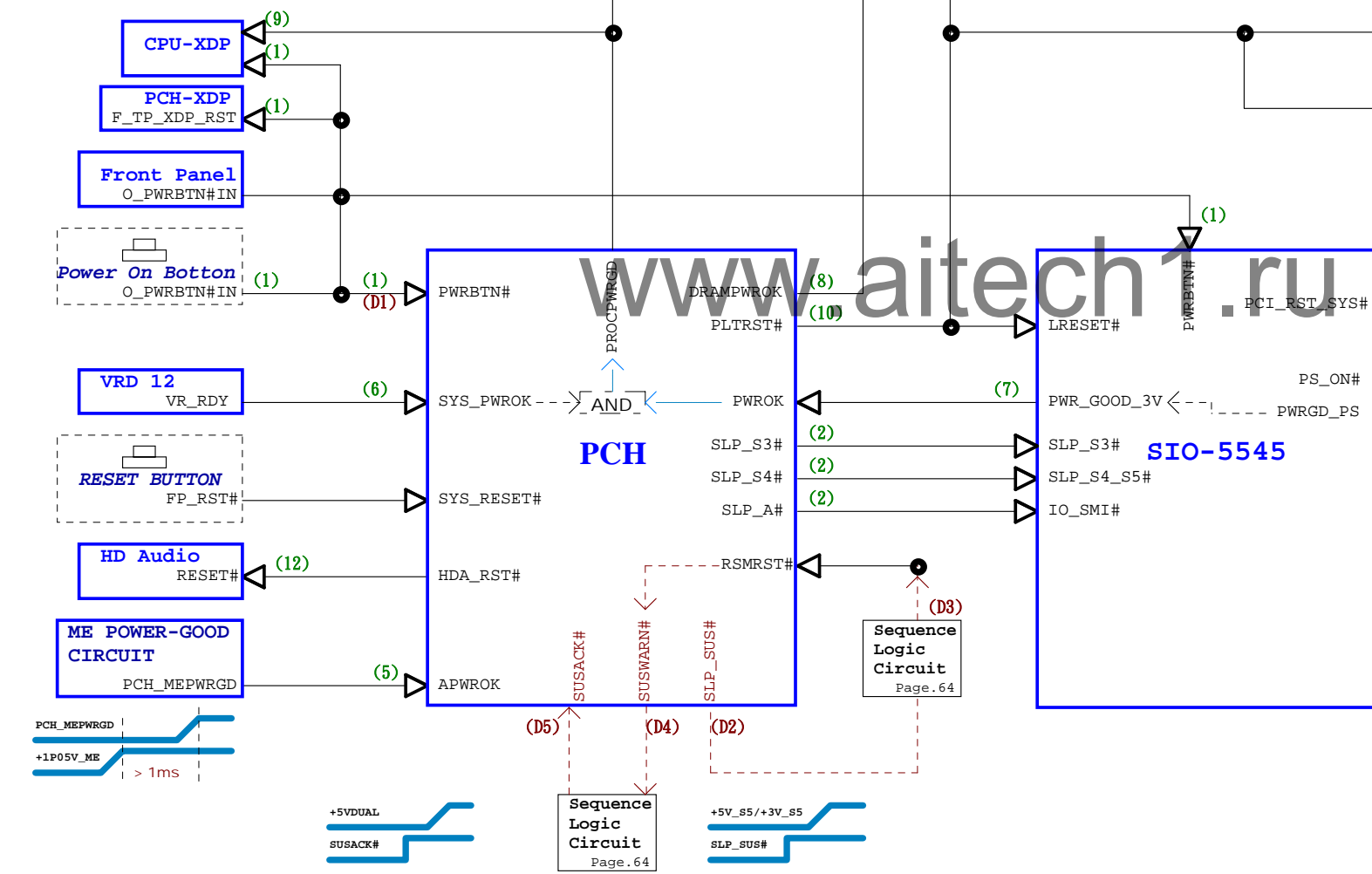
Timing diagram for the SWARN# signal. The diagram shows the SWARN# signal (purple) and other signals (DPWROK, PWR_ACK, P_SUS#, ISMRST#, -5VDUAL, +3V_85) over time. A vertical dashed line indicates a delay of 1.05µs between the SWARN# signal and the PWR_ACK signal.



RESET / Power Good MAP

Sequence Signal Name:

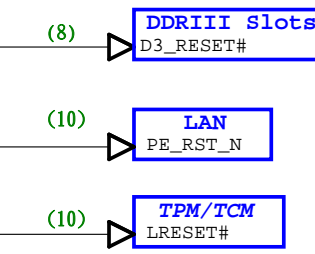
- (1) O_PWRBTN#IN
- (2) S_SLP_S4# S_SLP_S3# S_SLP_M#
- (3) O_PSON#
- (4) B_ATX_PWROK
- (5) PCH_MEPWRGD
- (6) S_PCH_SYSPWROK P_VR_READY
- (7) PWRGD_3V
- (8) H_DRAMPWROGD D3_RESET#
- (9) H_PWRGD
- (10) S_PLTRST# H_RESET#_R S_PLTRST#_R
- (11) X_PLTRST_PCIE_SLOT# K_PCIRST#_SLOT
- (12) A_Z_RST#



Deep Sleep Exit MAP

Sequence Signal Name:

- (D1) O_PWRBTN#IN
- (D2) S_SLP_SUS#
- (D3) S_RSMRST#
- (D4) S_SUSWARN#
- (D5) S_SUS_PWR_ACK#



IRQ Routing Table

| | INTA# | INTB# | INTC# | INTD# | IDSEL | REQn# | GNTn# |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Slot3 | C | D | A | B | 18 | 0 | 0 |

STRAPPING Table

CPU side

| CFG[17:0] | Description | |
|-----------|--|--|
| [2] | PCI Express static x16 lane numbering reversal | 1: normal Default 0: lane numbers reversed |
| [6:5] | PCI Express Bifurcation | 00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default |

| PIN NAME | NET | | Strapping description |
|---------------------|------------------|------|---|
| PCI2/TME (PIN4) | C_CK505_33M_PCI2 | 1 | Overclocking DISABLED DEFAULT |
| | | 0 | Overclocking ENABLED |
| PCI4/SRC5_EN (PIN6) | C_CK505_33M_PCI4 | 1 | SRC5 DEFAULT |
| | | 0 | CPU_STOP# and PCI_STOP# |
| PCIF5/ITP_EN (PIN7) | C_CK505_33M_PCI5 | 1 | CPU_ITP |
| | | 0 | SRC8 DEFAULT |
| PCI3/CFGF (PIN5) | C_CK505_33M_PCI3 | LOW | See CFG Table DEFAULT (Set SATA and SRC come from PLL4) |
| | | Mid | See CFG Table |
| | | High | See CFG Table |

SIO SMSC5545

| PIN NAME | NET | | Strapping description |
|---------------------------------|-----------|---|---|
| GP070 / PWM4 (PIN127) | O_SPEAKER | 1 | Diag_En Disable |
| | | 0 | Diag_En Enable DEFAULT |
| DTR1# [TEST_EN] /GP051 (PIN104) | O_DTR1#_R | 1 | PE BOOT Loader Strap (DTR1#)= Load from SPI |
| | | 0 | PE BOOT Loader Strap (DTR1#)= No Load from SPI DEFAULT |

PCH

On-Die PLL Voltage Regulator Voltage Select

| HDA_SYNC | Description | |
|----------|-------------|----------------|
| High | 1.5V | DEFAULT |
| Low | 1.8V | |

On-Die PLL Voltage Regulator

| GPIO28 (IN-PU) | Description | |
|----------------|------------------------|----------------|
| High | Regulator is enabled. | DEFAULT |
| Low | Regulator is disabled. | |

Topblock Swap Mode

| GNT3#/GPIO55 (IN-PU) | Description | |
|----------------------|-----------------------------|----------------|
| High | Topblock swap mode: Disable | DEFAULT |
| Low | Topblock swap mode: Enable | |

No Reboot Mode

| SPKR (IN-PD) | Description | |
|--------------|-------------------------|----------------|
| High | No reboot mode: Enable | DEFAULT |
| Low | No reboot mode: Disable | |

Integrated 1.05V VRM

| INTVRMEN | Description | |
|----------|-------------------------------|----------------|
| High | Integrated 1.05V VRM: Enable | DEFAULT |
| Low | Integrated 1.05V VRM: Disable | |

TLS Confidentiality

| GPIO15 (IN-PD) | Description | |
|----------------|--|----------------|
| High | ME Crypto TLS cipher suite with confidentiality | DEFAULT |
| Low | ME Crypto TLS cipher suite with no confidentiality | |

Flash Descriptor Override Strap

| HDA_SDO | Description | |
|---------|--|----------------|
| High | Flash descriptor security will be override | DEFAULT |
| Low | Disable ME in Manufacturing Mode | |

DMI Rx Termination Voltage

| SPI_MOSI (IN-PD) | Description | |
|------------------|----------------------------|----------------|
| Low | DMI Rx Termination Voltage | DEFAULT |

DMI Termination Voltage

| NV_CLE (IN-PU) | Description | |
|----------------|---------------------------------------|----------------|
| High | DMI and FDI Tx/Rx Termination Voltage | DEFAULT |

Boot BIOS Destination Selection

| GNT1# (IN-PU) | SATA1GP/GP19 (IN-PU) | Description | |
|---------------|----------------------|----------------------------|----------------|
| Low | Low | Flash cycle routed to LPC | DEFAULT |
| High | Low | Flash cycle routed to PCI | |
| Low | High | Flash cycle routed to NAND | |
| High | High | Flash cycle routed to SPI | |

Deep S4/S5 Well on-die Voltage Regulator Enable

| DSWVRMEN | Description | |
|----------|-------------|----------------|
| High | Enable | DEFAULT |
| Low | Disable | |

Digital Port C Strap

| DDPC_CTRLDATA | Description | |
|---------------|------------------|----------------|
| High | Configure Port C | DEFAULT |
| Low | Disable | |



Title
GPIO/IRQ/IDSEL Table

DWG NO
Lanikai_MT/DT

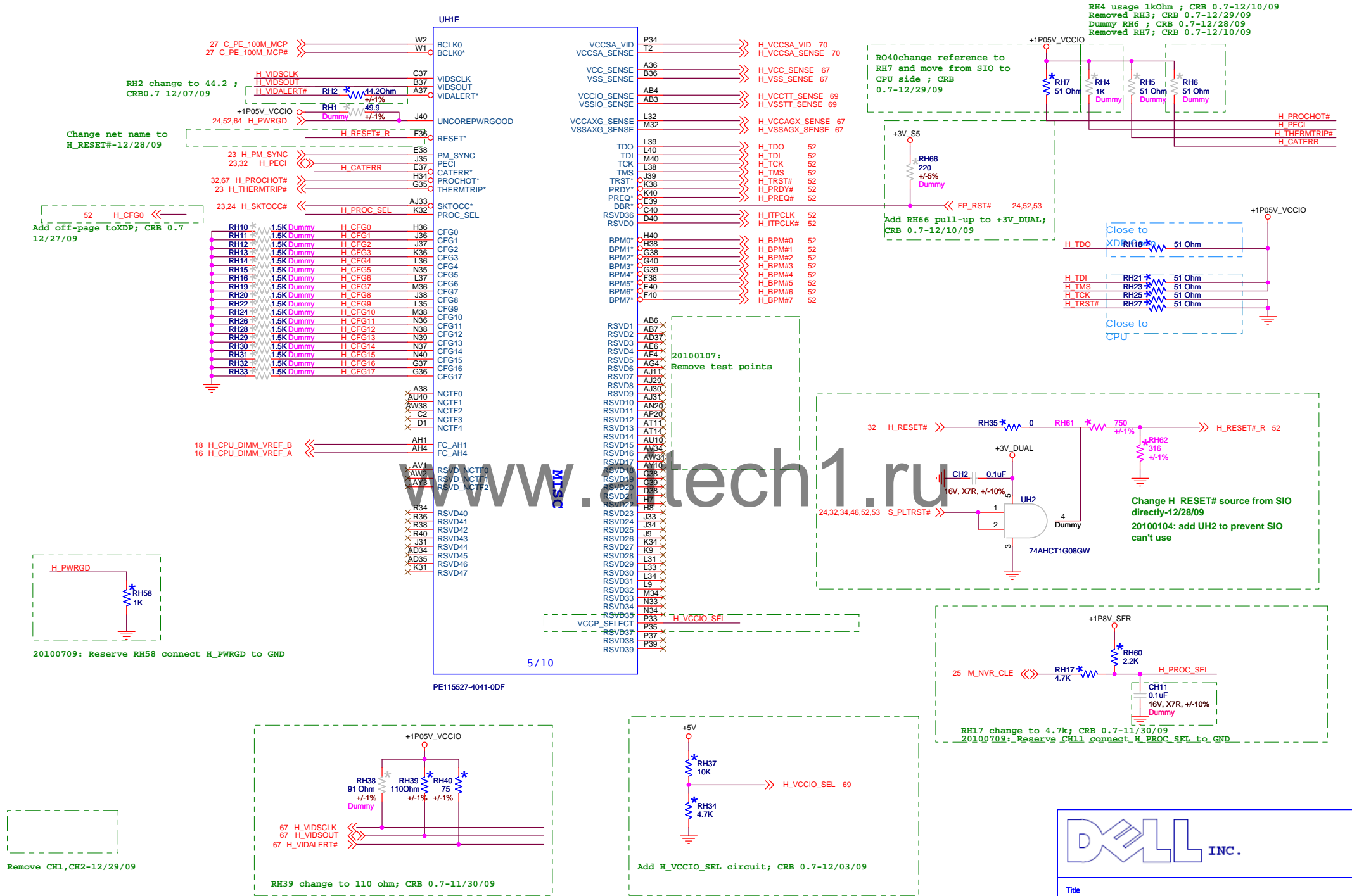
Date: Wednesday, June 13, 2012 Sheet 7 of 71

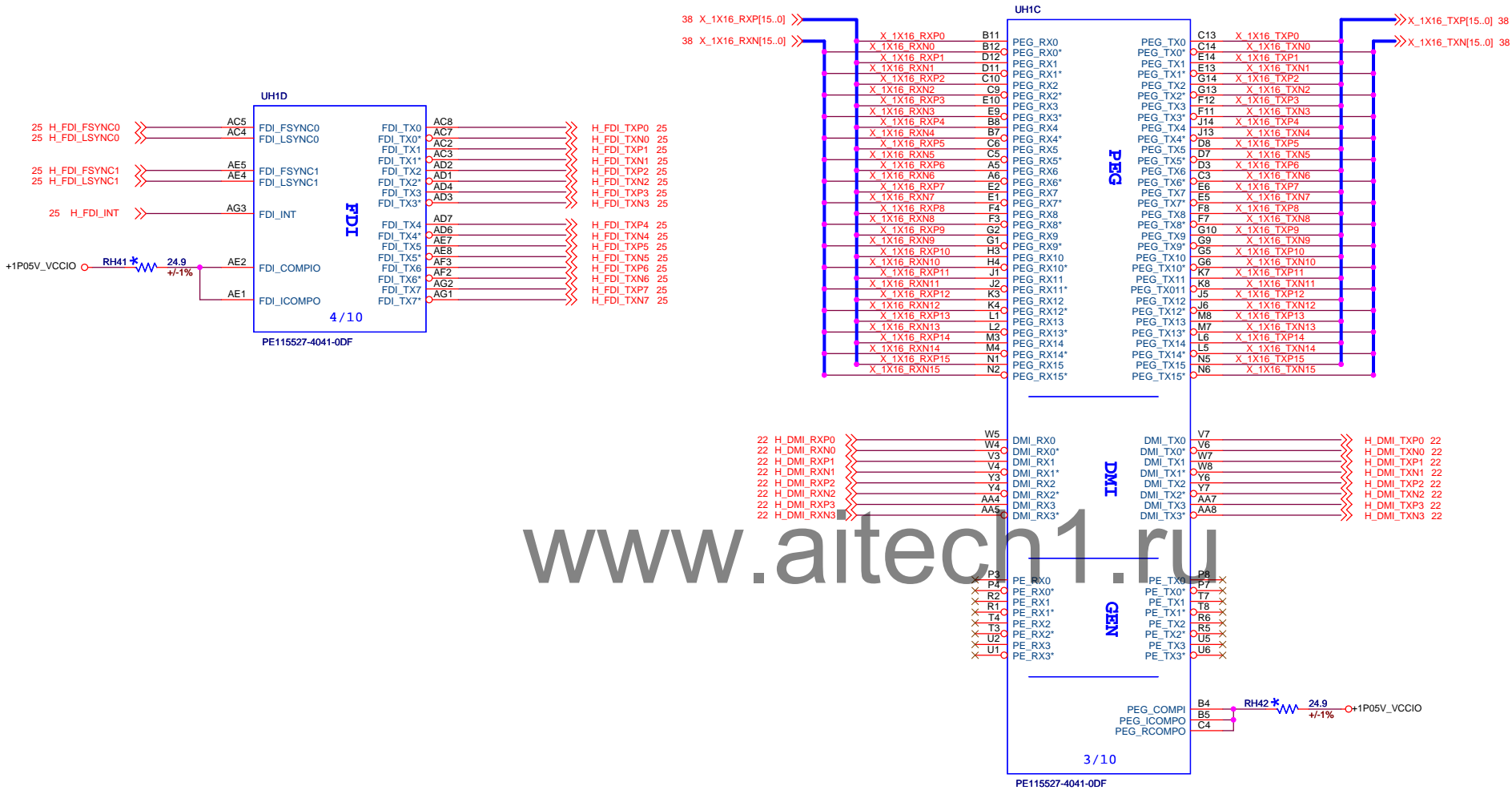
| PCH GPIO Summary | | | | | | |
|------------------|------|------------|---------|---------------------------|--|-------------------------|
| GPIO | Type | Power Well | Default | IN-PU/PD | EX-PU/PD | Schematic Usage |
| GPIO[0] | IO | Core | GPI | -- | 10k pull-up to +3V | S_PECI_REG# |
| GPIO[1] | IO | Core | GPI | 20K IN-PU (only on TACH1) | 10k pull-up to +3V (dummy) 1k pull-down to GND | S_OPL_CHASSIS_ID0 |
| GPIO[2] | IOD | Core | GPI | -- | 8.2k pull-up to +3V | PCIE_MINI_CPUSS_DETECT# |
| GPIO[3] | IOD | Core | GPI | -- | -- | V_DDSF_C_HPD |
| GPIO[4] | IOD | Core | GPI | -- | 8.2k pull-up to +3V | V_GPL_VGA_CBL_DET# |
| GPIO[5] | IOD | Core | GPI | -- | 8.2k pull-up to +3V | PCIE_MINI_CPPE_DETECT# |
| GPIO[6] | IO | Core | GPI | 20K IN-PU (only on TACH2) | 10k pull-up to +3V | S_OPL_PCH_HS_DET# |
| GPIO[7] | IO | Core | GPI | 20K IN-PU (only on TACH3) | 10k pull-up to +3V (dummy) 220 pull-down to GND | S_OPL_SKU2 |
| GPIO[8] | IO | Suspend | GPO | 20K IN-PU | -- | S_TP_0P8 |
| GPIO[9] | IO | Suspend | Native | -- | 8.2k pull-up to +3V_S5 (dummy) | U_USB_OC_R_#5 |
| GPIO[10] | IO | Suspend | Native | -- | 10k pull-up to +3V_S5 | X_WLAN_WAKE# |
| GPIO[11] | IO | Suspend | Native | -- | 10k pull-up to +3V_S5 | X4_WAKE# |
| GPIO[12] | IO | Suspend | Native | -- | 10k pull-up to +3V_LAN 10k pull-down to GND (dummy) | L_LAN_DISABLE# |
| GPIO[13] | IO | Suspend | GPI | -- | 10k pull-up to +3V_S5 | X1_WAKE# |
| GPIO[14] | IO | Suspend | Native | -- | 8.2k pull-up to +3V_S5 | GPO_WLOM |
| GPIO[15] | IO | Suspend | GPO | 20K IN-PD | 1k pull-up to +3V_S5 (dummy) | S_PCH_GP15 |
| GPIO[16] | IO | Core | GPI | -- | 10k pull-up to +3V 10k pull-down to GND (dummy) | H_SKT0CC_R_# |
| GPIO[17] | IO | Core | GPI | 20K IN-PU (only on TACH0) | 10k pull-up to +3V (dummy) 1k pull-down to GND | S_OPL_CHASSIS_ID1 |
| GPIO[18] | IO | Core | GPI | 20K IN-PU | 1k pull-up to +3V (dummy) 1k pull-down to GND (dummy) | S_SATA10P |
| GPIO[19] | IO | Core | Native | -- | 10k pull-up to +3V 10k pull-down to GND (dummy) | S_FLEXBAY_HDR_CBL_DET# |
| GPIO[20] | IO | Core | GPI | -- | 10k pull-up to +3V (dummy) 10k pull-down to GND | S_OPL_BRD_REV0 |
| GPIO[21] | IO | Core | GPI | -- | 1k pull-up to +3V 4.7k pull-down to GND (dummy) | S_PCH_CONFIG_JUMPER |
| GPIO[22] | IO | Core | Native | 20K IN-PU | 10k pull-up to +3V (dummy) | L_DRG1# |
| GPIO[24] | IO | Suspend | GPO | -- | 100k pull-up to +3V_S5 | H_SKT0CC# |
| GPIO[27] | IO | Deep Sleep | GPI | 20K IN-PU | 10k pull-up to +3V_DUAL 1k pull-down to GND (dummy) | S_OP27_PD |
| GPIO[28] | IO | Suspend | GPO | 20K IN-PU | 10k pull-up to +3V_S5 1k pull-down to GND (dummy) | S_PCH_GP28_PU |
| GPIO[29] | IO | Suspend | Native | -- | 1k pull-up to +3V_S5 (dummy) | S_SLP_LAN# |
| GPIO[30] | IO | Deep Sleep | Native | -- | 10k pull-up to +3V_DUAL (dummy) 1k pull-down to GND (dummy) | S_SUSWARN# |
| GPIO[31] | IO | Deep Sleep | GPI | TBD IN-PD | 8.2k pull-up to +3V_DUAL | S_PSWD_CLR |
| GPIO[32] | IO | Core | GPO | -- | 10k pull-up to +3V (dummy) 220 pull-down to GND | S_OPL_SKU0 |
| GPIO[33] | IO | Core | GPO | -- | -- | -- |
| GPIO[34] | IO | Core | GPI | -- | 10k pull-up to +3V | PCH_GPIO34 |
| GPIO[35] | IO | Core | GPO | -- | 10k pull-up to +3V (dummy) 220 pull-down to GND | S_OPL_SKU1 |
| GPIO[36] | IO | Core | GPI | 20K IN-PD | -- | S_PCH_GP36 |
| GPIO[37] | IO | Core | GPI | 20K IN-PD | -- | S_PCH_GP37 |
| GPIO[38] | IO | Core | GPI | -- | 10k pull-up to +3V (dummy) 10k pull-down to GND | S_OPL_CHASSIS_ID2 |
| GPIO[39] | IO | Core | GPI | -- | 10k pull-up to +3V | A_FP_PRES# |
| GPIO[40] | IO | Suspend | Native | -- | -- | U_USB_OC_R_#1 |

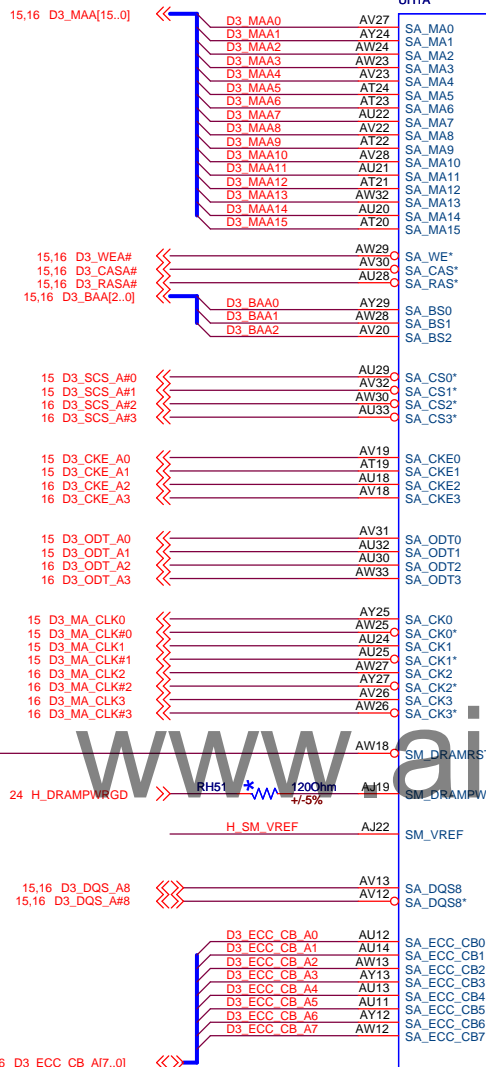
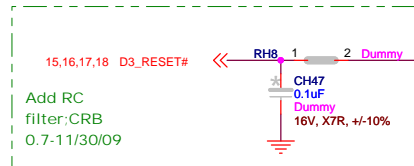
| | | | | | | |
|----------|-----|---------|----------------------|---------------------------|--|------------------------|
| GPIO[41] | I/O | Suspend | Native | -- | -- | U_USB_OC_R_#2 |
| GPIO[42] | I/O | Suspend | Native | -- | -- | U_USB_OC_R_#3 |
| GPIO[43] | I/O | Suspend | Native | -- | 8.2k pull-up to +3V_S5 (dummy) | U_USB_OC_R_#4 |
| GPIO[44] | I/O | Suspend | Native | 20k IN-PU | 10k pull-up to +3V_S5 10k pull-down to GND (dummy) | S_INTRUD_CBL_DET# |
| GPIO[45] | I/O | Suspend | Native | -- | 10k pull-up to +3V_S5 10k pull-down to GND (dummy) | O_COM_SER2_DET# |
| GPIO[46] | I/O | Suspend | Native | 20k IN-PU | 10k pull-up to +3V_S5 (dummy) 1k pull-down to GND | S_OPL_BRD_REV1 |
| GPIO[48] | I/O | Core | GPI | -- | 10k pull-up to +3V | S_OPIO48_PU |
| GPIO[49] | I/O | Core | GPI | -- | 8.2k pull-up to +3V | TMIN_SHIFT |
| GPIO[50] | I/O | Core | Native | -- | 8.2k pull-up to +3V | K_REQ#1 |
| GPIO[51] | I/O | Core | Native | 20k IN-PU | 1k pull-up to +3V (dummy) 1k pull-down to GND (dummy) | K_ONT#1 |
| GPIO[52] | I/O | Core | Native | -- | 8.2k pull-up to +3V | K_REQ#2 |
| GPIO[53] | I/O | Core | Native | 20k IN-PU | 1k pull-down to GND (dummy) | K_ONT#2 |
| GPIO[54] | I/O | Core | Native | -- | 8.2k pull-up to +3V | K_REQ#3 |
| GPIO[55] | I/O | Core | Native | 20k IN-PU | 1k pull-down to GND (dummy) | K_ONT#3 |
| GPIO[57] | I/O | Suspend | GPI | -- | 10k pull-up to +3V_S5 (dummy) 47k pull-down to GND | S_OPIO57_PD |
| GPIO[58] | I/O | Suspend | Native | -- | 10k pull-up to +3V_S5 | S_SMLINK1_CLK |
| GPIO[59] | I/O | Suspend | Native | -- | -- | U_USB_OC_R_#0 |
| GPIO[60] | I/O | Suspend | Native | -- | 2.2k pull-up to +3V_S5 | GPIO_WIRELESS_DISABLE# |
| GPIO[61] | I/O | Suspend | Native | -- | 8.2k pull-up to +3V_S5 (dummy) | S_LPCPD# |
| GPIO[62] | I/O | Suspend | Native | -- | -- | S_SUSCLK |
| GPIO[63] | I/O | Suspend | Native | -- | 10k pull-up to +3V_S5 | S_PCIAUX_GATE |
| GPIO[64] | I/O | Core | Native | 20k IN-PD | -- | S_TP_CLKOUTFLEX0 |
| GPIO[65] | I/O | Core | Native | 20k IN-PD | -- | C_14M_SIO_R |
| GPIO[66] | I/O | Core | Native | 20k IN-PD | -- | S_TP_CLKOUTFLEX2 |
| GPIO[67] | I/O | Core | Native | 20k IN-PD | -- | C_14M_TMR_R |
| GPIO[68] | I/O | Core | GPI | 20k IN-PU (only on TACH4) | 10k pull-up to +3V (dummy) 220 pull-down to GND | S_OPL_BRD_REV2 |
| GPIO[69] | I/O | Core | GPI | 20k IN-PU (only on TACH5) | 10k pull-up to +3V | O_PRT_DET# |
| GPIO[70] | I/O | Core | Native | 20k IN-PU (only on TACH6) | 8.2k pull-up to +3V | S_FP_CHAS_DET# |
| GPIO[71] | I/O | Core | Native | 20k IN-PU (only on TACH7) | 10k pull-up to +3V | -- |
| GPIO[72] | I/O | Suspend | Native (Mobile Only) | 20k IN-PU | 10k pull-up to +3V_S5 | S_PCH_GP72_PU |
| GPIO[74] | I/O | Suspend | Native | -- | 10k pull-up to +3V_S5 | S_MFG_MODE_OR |
| GPIO[75] | I/O | Suspend | Native | -- | 10k pull-up to +3V_S5 | S_SMLINK1_DATA |

| GPIO | PIN NAME | Power well | Buffer Type | EX-PU/PD | Signal Name |
|-------|-------------------------------------|------------|--------------|---|--------------------|
| OP000 | (DIA0_LED0#) OP000 | VTR | I/O | NA | O_DIA0_LED0# |
| OP001 | (DIA0_LED1#) OP001 | VTR | I/O | NA | O_DIA0_LED1# |
| OP002 | (DIA0_LED2#) OP002 | VTR | I/O | NA | O_DIA0_LED2# |
| OP003 | (DIA0_LED4#) OP003 | VTR | I/O | NA | O_DIA0_LED4# |
| OP004 | OP004 | VTR | I/O | NA | NC |
| OP005 | (H_CUPRST#) OP005 / PECIAL_REQUEST# | VTR | IO/OD | 10k pull-up to +3V | O_PECIAL_REQUEST# |
| OP006 | YELLOW# / OP006 | VTR | OD/O | NA | O_YELLOW# |
| OP007 | GREEN# / OP007 | VTR | OD/O | NA | O_GREEN# |
| OP010 | SMODAT2 / OP010 | VTR | IODIO | 0.2k pull-up to +3V_DUAL (dummy) | S_SMLINK1_DATA_R |
| OP011 | SMBCLK2 / OP011 | VTR | IODIO | 8.2k pull-up to +3V_DUAL (dummy) | S_SMLINK1_CLK_R |
| OP012 | OP012 | VTR | I/O | 8.2k pull-up to +3V_DUAL | SPL_DI |
| OP013 | OP013 | VTR | I/O | NA | NC |
| OP014 | (TMIN_SHIFT) OP014 | VTR | I/O | 8.2k pull-up to +3V | TMIN_SHIFT |
| OP015 | PWRBTN# / OP015 | VTR | I/O | 1k pull-up to +3V_DUAL | O_PWRBTN# |
| OP016 | PROCHOT_J# / PROCHOT_OUT# / OP016 | VTR | IODIOD | 51 ohm pull-up to +1P05V_VCCIO | H_PROCHOT# |
| OP017 | TACH1 / OP017 | VTR | I/O | 1k pull-up to +3V | O_SEN_CPUFAN |
| OP020 | TACH2 / OP020 | VTR | I/O | 1k pull-up to +3V | O_SEN_CHAFAN |
| OP021 | TACH3 / OP021 | VTR | I/O | NA | NC |
| OP022 | PWM1 / OP022 | VTR | OD/O | 4.7k pull-up to +3V | O_CPUFAN_PWM |
| OP023 | PWM2 / OP023 | VTR | OD/O | 4.7k pull-up to +3V | O_CHAFAN_PWM |
| OP024 | PWM3 / OP024 | VTR | OD/O | NA | NC |
| OP025 | (FP_CBL_DET#) OP025 | VTR | I/O | 8.2k pull-up to +3V_S5 | O_FP_CBL_DET# |
| OP026 | PCL_RST_S5# / OP026 | VTR | OD/O | NA | X_PLTRST_PCL_SL0T# |
| OP027 | PCL_RST_SL0T# / OP027 | VTR | OD/O | NA | H_RESET# |
| OP030 | PS_ON# / OP030 | VTR | OD/O | 4.7k pull-up to +5VSB | O_PSON# |
| OP031 | (PC_SPHR_DET) OP031 | VTR | I/O | 8.2k pull-up to +3V_DUAL | O_AUD_PCSPHR_DET# |
| OP032 | OP032 | VTR | I/O | NA | NC |
| OP033 | PWR_GOOD_3V / OP033 | VTR | OD/O | NA | PWRGD_3V |
| OP034 | RSNRST# / OP034 | VTR | OD/O | 10k pull-down to GND | O_RSNRST# |
| OP035 | OP035 | VTR | I/O | 8.2k pull-up to +3V_DUAL | O_BC_CLK |
| OP036 | (OP036 / SMB_CLK1) | VTR | IO/OD | 8.2k pull-up to +3V_DUAL (dummy) | S_SMBCLK_PCL_R |
| OP040 | (OP040 / SMB_DAT1) | VTR | IO/OD | 8.2k pull-up to +3V_DUAL (dummy) | S_SMBDATA_PCL_R |
| OP041 | OP041 / IO_FME# | VTR | IO/OD | 10k pull-up to +3V_S5 | O_IO_FME# |
| OP042 | OP042 / DRV0EN0 | VTR | IO/IO | 100k pull-up to +3V_DUAL (dummy) | T_ESATA_DET# |
| OP043 | DCD1# / OP043 / MCDAT | VTR | IO/IO | NA | O_DCD1#_R |
| OP044 | DSR1# / OP044 / MCLK | VTR | IO/IO | NA | O_DSR1#_R |
| OP045 | ROD1 / OP045 | VTR | I/O | NA | O_ROD1_R |
| OP046 | RTS1# / OP046 | VTR | OD/O | NA | O_RTS1#_R |
| OP047 | (SV_PSRNT) OP047 / THD1 | VTR | IO/IO | NA | O_THD1_R |
| OP050 | CTS1# / OP050 | VTR | I/O | NA | O_CTS1#_R |
| OP051 | DTR1# / TEST_EN# / OP051 | VTR | OD/O | 8.2k pull-up to +3V_DUAL (dummy) 30k pull-down to GND | O_DTR1#_R |
| OP052 | R11# / OP052 | VTR | I/O | NA | O_R11#_R |
| OP053 | OP053 / DCD2# | VTR | IO/O | 2.2k pull-up to +3V | O_DCD2#_R |
| OP054 | OP054 / DSR2# | VTR | IO/O | 2.2k pull-up to +3V | O_DSR2#_R |
| OP055 | OP055 / ROD2 | VTR | IO/O | 2.2k pull-up to +3V | O_ROD2_R |
| OP056 | (PWR2_PSRNT) OP056 / RTS2# | VTR | IO/IO | 30k pull-up to +3V | O_RTS2#_R |
| OP057 | (MB_RE0_P0) OP057 / TXD2 | VTR | IO/IO | 30k pull-up to +3V | O_TXD2_R |
| OP060 | OP060 / CTS2# | VTR | IO/O | 2.2k pull-up to +3V | O_CTS2#_R |
| OP061 | (MEM_RE0_P0) OP061 / DTR2# | VTR | IO/IO | 30k pull-up to +3V | O_DTR2#_R |
| OP062 | OP062 / R12# | VTR | IO/O | 2.2k pull-up to +3V | O_R12#_R |
| OP063 | OP063 / XBORST# | VTR | IO/OD | 10k pull-up to +3V | O_XBORST# |
| OP064 | OP064 / A20M | VTR | IO/OD | 10k pull-up to +3V | O_A20M |
| OP065 | SLP_S3# / OP065 | VTR | I/O | NA | S_SLP_S3# |
| OP066 | SLP_S4_S5# / OP066 | VTR | I/O | NA | S_SLP_S4# |
| OP067 | PWR0D_PS1 / OP067 | VTR | I/O | 1k pull-up to +5V | B_ATT_PWROK |
| OP070 | SPEAKER [DIA0_EN#] / OP070 | VTR | OD/O | 8.2k pull-up to +3V_DUAL (dummy) 8.2k pull-down to GND | O_SPEAKER |
| OP071 | (SLP_M#) OP071 / IO_SMI# | VTR | IO/OD | NA | S_SLP_M# |
| OP072 | PECL1 / LVSBM_CLK1 / OP072 | VTR | PECL/IO/ODIO | 1k pull-up to +1P05V_VCCIO (dummy) | H_PEC1_R |
| OP073 | PECL_READY / LVSBM_DAT1 / OP073 | VTR | PECL/IO/ODIO | 1k pull-up to +1P05V_VCCIO | O_OP73_PU |

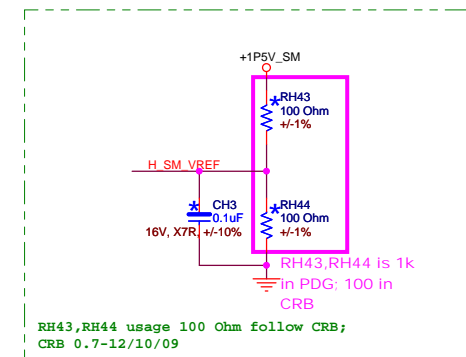
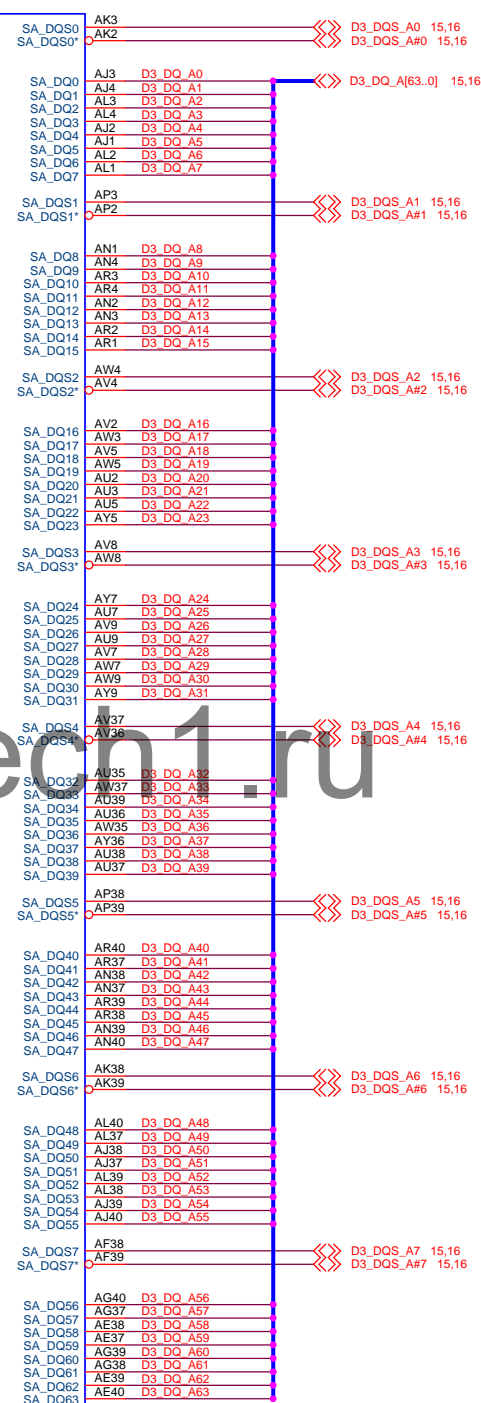








DDR_A



DELL INC.

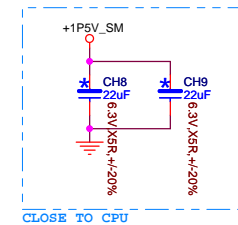
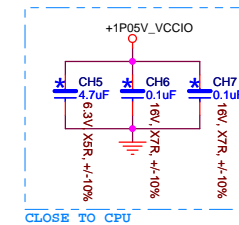
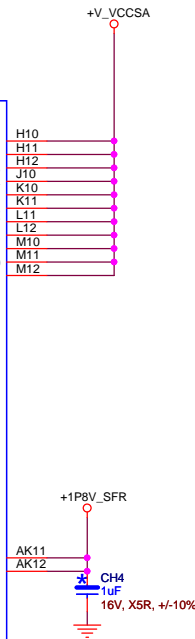
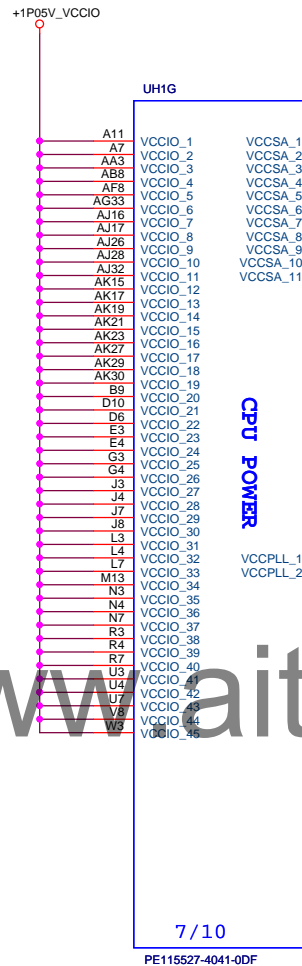
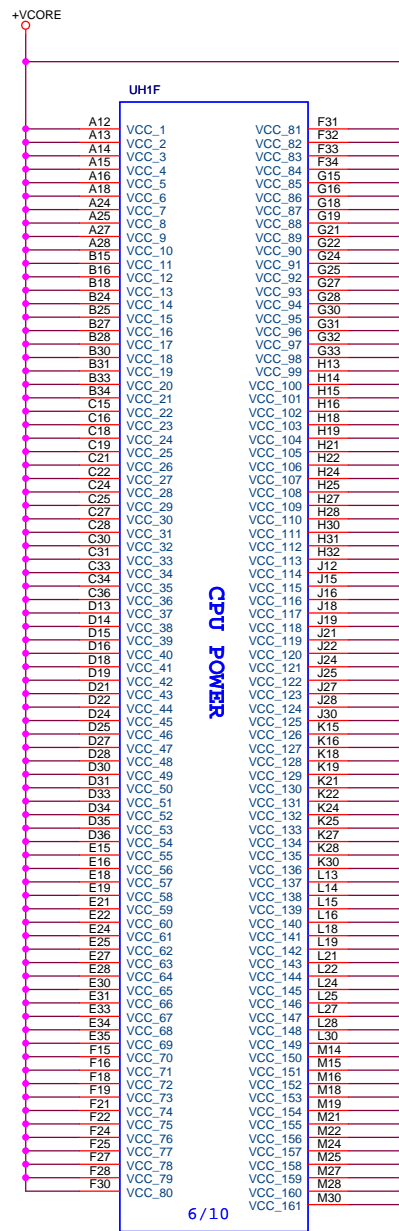
Title: **CPU-3: DDR3_CHA**

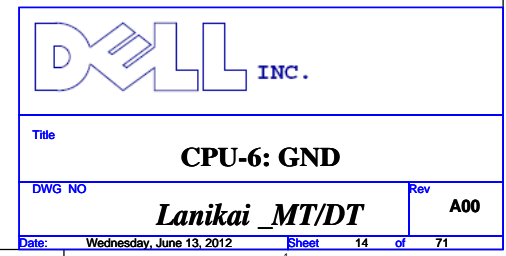
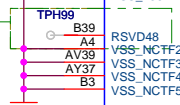
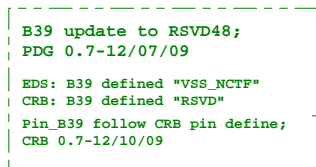
DWG NO: **Lanikai_MT/DT** Rev: **A00**

Date: **Wednesday, June 13, 2012** Sheet: **11** of **71**

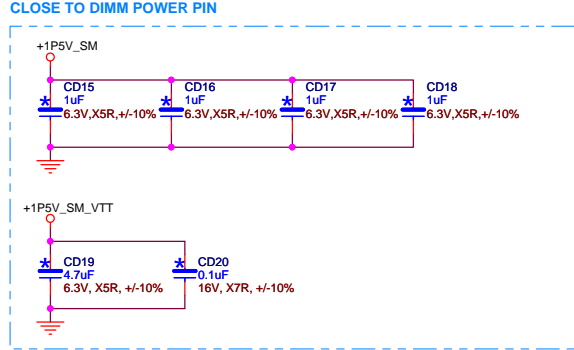
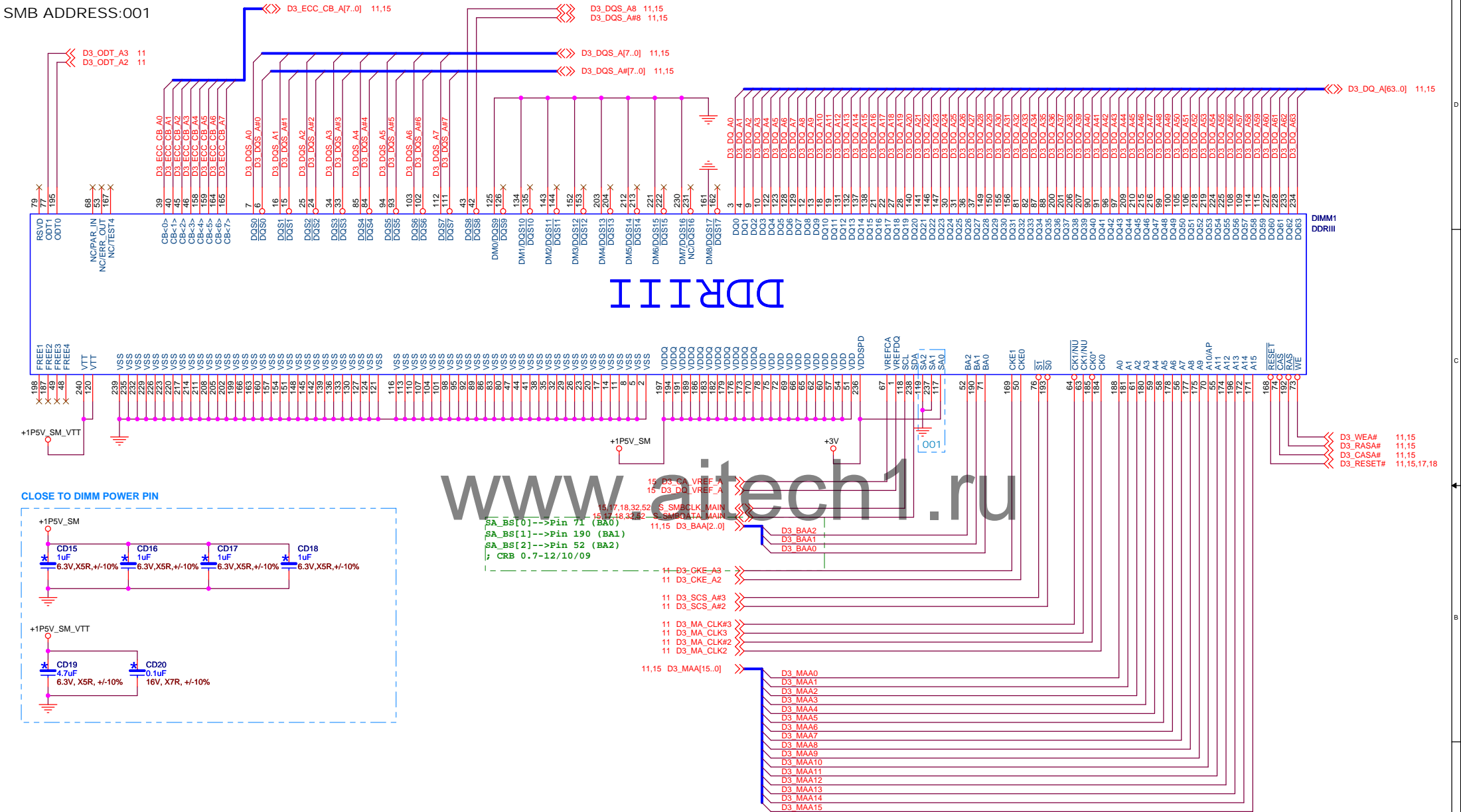
PE115527-4041-0DF

1 / 10

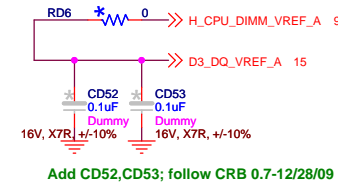





CHANNEL A BANK 2
SMB ADDRESS:001



SA_BS[0]-->Pin 71 (BA0)
SA_BS[1]-->Pin 190 (BA1)
SA_BS[2]-->Pin 52 (BA2)
; CRB 0.7-12/10/09



INC.

Title

DDR3 Conn: CHA_2 (DIMM1)

DWG NO

Lanikai MT/DT

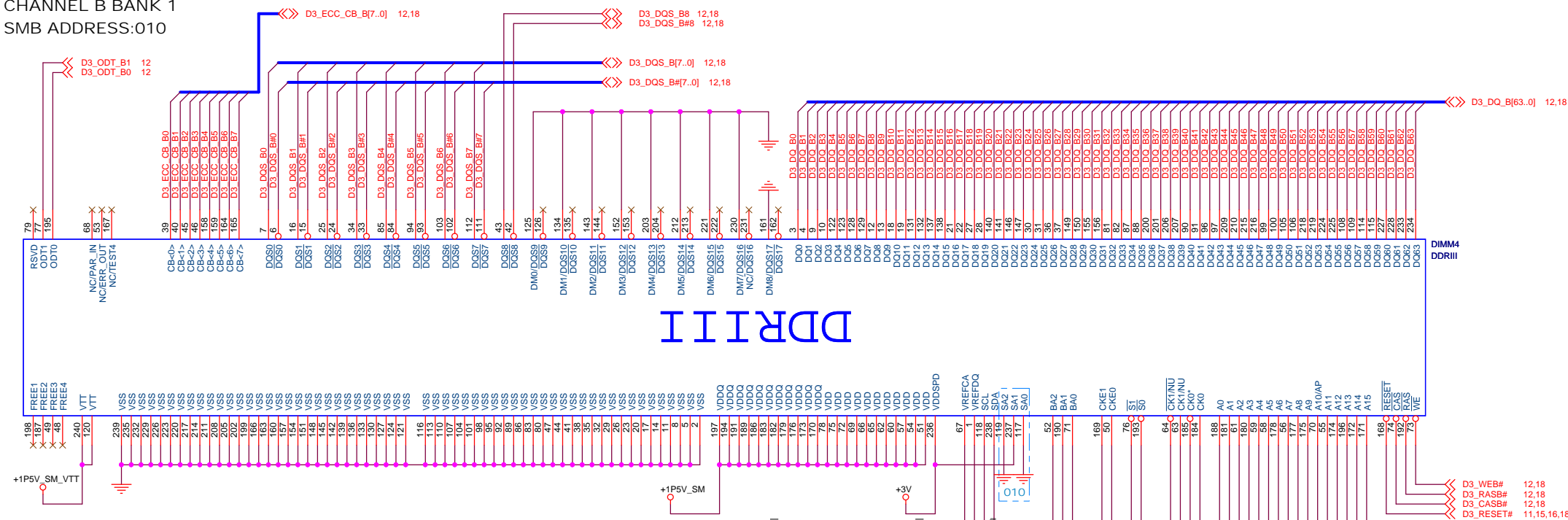
Rev

A00

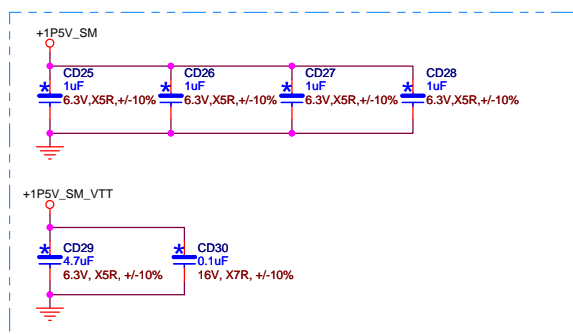
Date: Wednesday, June 13, 2012

Sheet 16 of 71

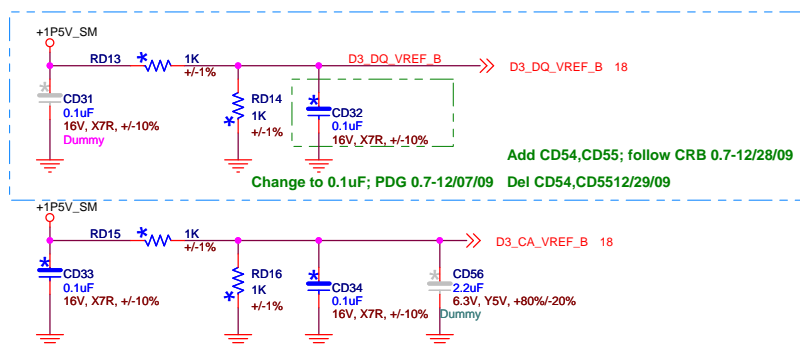
CHANNEL B BANK 1
SMB ADDRESS:010



CLOSE TO DIMM POWER PIN



PLACE CLOSE TO CH-B DIMM



Title

DDR3 Conn: CHB_1 (DIMM4)

| | |
|--------|--|
| DWG NO | |
|--------|--|

Lanikai MT/DT

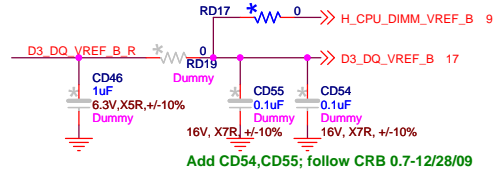
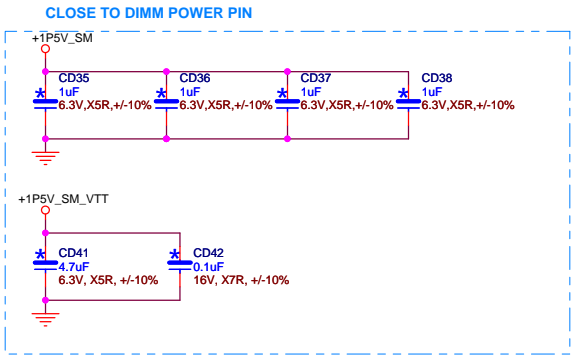
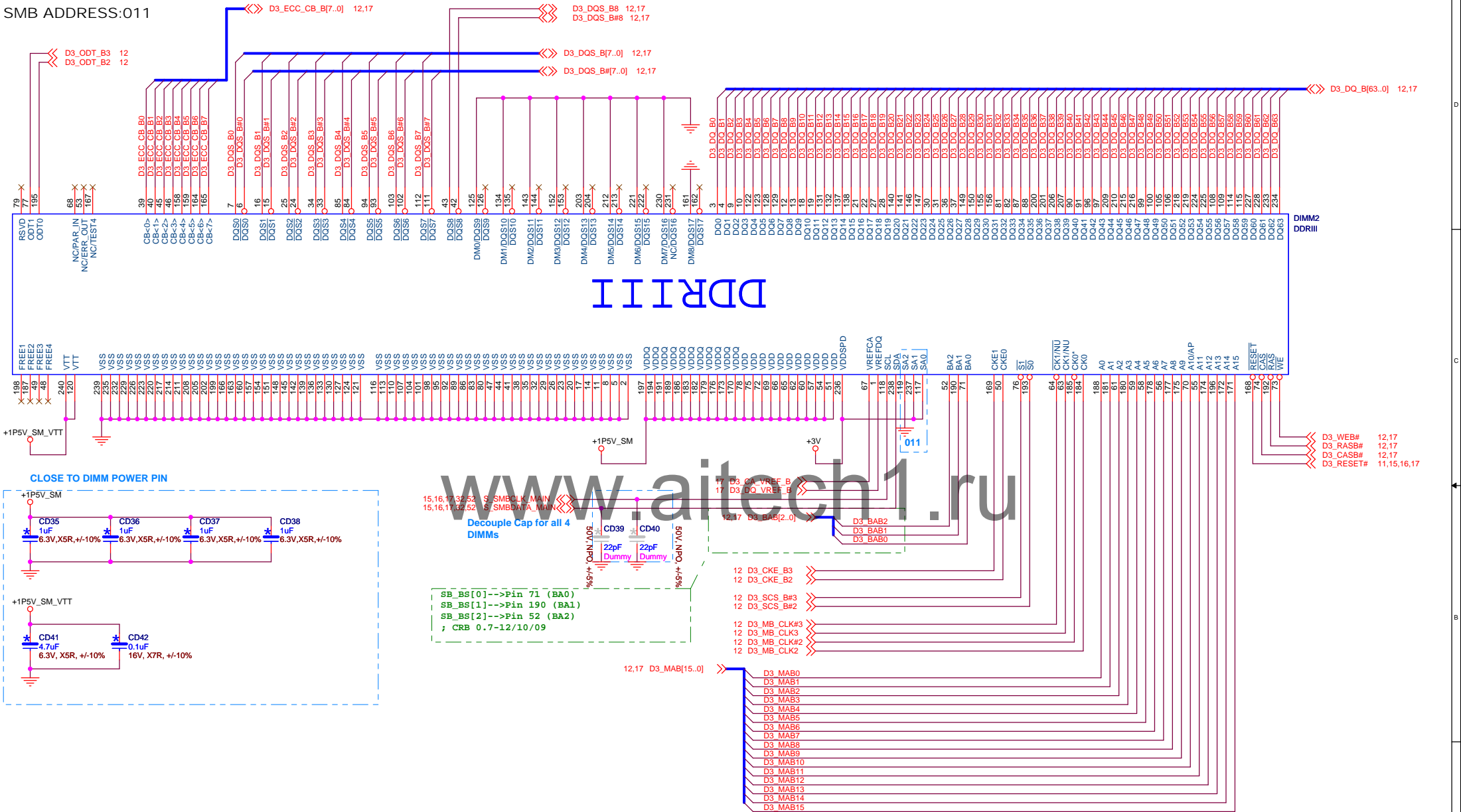
Rev


A00

Date: Wednesday, June 13, 2012

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CHANNEL B BANK 2
SMB ADDRESS:011





INC.

Title

DDR3 Conn: CHB_2 (DIMM2)

DWG NO

Lanikai MT/DT

Date: Wednesday, June 13, 2012

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Sheet 18 of 71

20100106: Remove ONFI function since not support

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Title
TBD

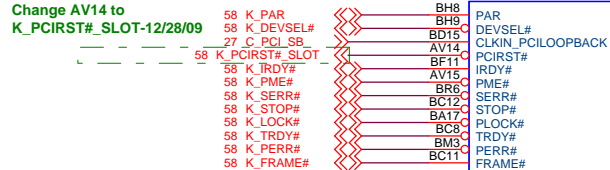
| | | | |
|--------|----------------------|-----|------------|
| DWG NO | Lanikai_MT/DT | Rev | A00 |
|--------|----------------------|-----|------------|

| | | | | | |
|-------|--------------------------|-------|----|----|----|
| Date: | Wednesday, June 13, 2012 | Sheet | 19 | of | 71 |
|-------|--------------------------|-------|----|----|----|

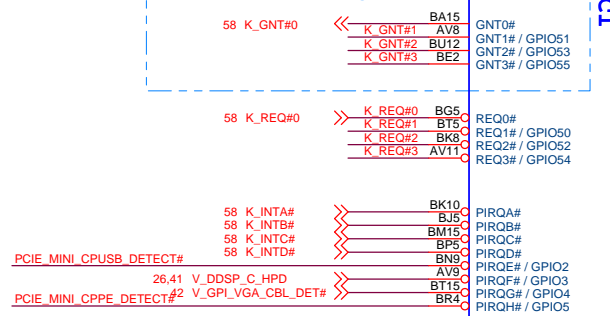
www.aitech1.ru

| | | |
|---|----------------------|---------|
|  | | |
| Title | | |
| Clock GEN | | |
| DWG NO | <i>Lanikai_MT/DT</i> | Rev A00 |
| Date: Wednesday, June 13, 2012 | Sheet 20 | of 71 |

Change AV14 to
K_PCIRST#_SLOT-12/28/09



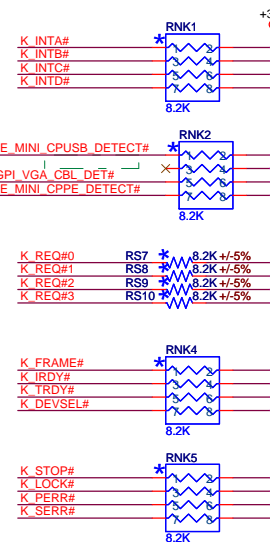
GNT [3:0] have Internal Pull-High to 3.3V



PCIE_MINI_CPUSB_DETECT#
26.41 V_DDSP_C_HPD
PCIE_MINI_CPPE_DETECT#2 V_GPI_VGA_CBL_DET#



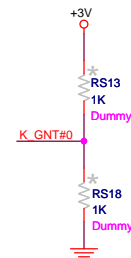
K_INTF# change to
V_DDSP_C_HPD-12/30/09
20100108: Remove
V_DDSP_C_HPD pull-up



K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_PME# add RS198 to
pull-up +3V_PCIAUX;
20100108: Remove
Dummy RS198;

PDG 0-8



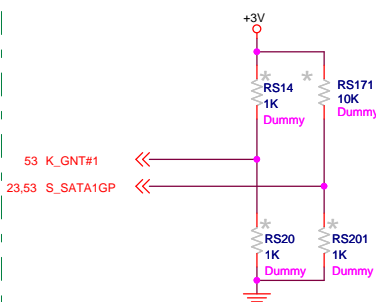
www.aitech1.ru

Left biotth SATA/GPIO19 and GNT1# floating.
No pull up required for Default(SPI)

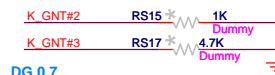
20091209: Have to check with
20091230: Reserved RS171
and RS201 for Boot select

Boot BIOS Select

| Boot Device | GNT1 | SATA1GP |
|-------------|------|---------|
| LPC | 0 | 0 |
| PCI | 1 | 0 |
| NAND | 0 | 1 |
| SPI | 1 | 1 |



GNT3# Internal pull-up.



DG 0.7
GNT3 is top block swap mode:
connect to ground with 4.7k ohm weak
pull down resistor for top block swap mode

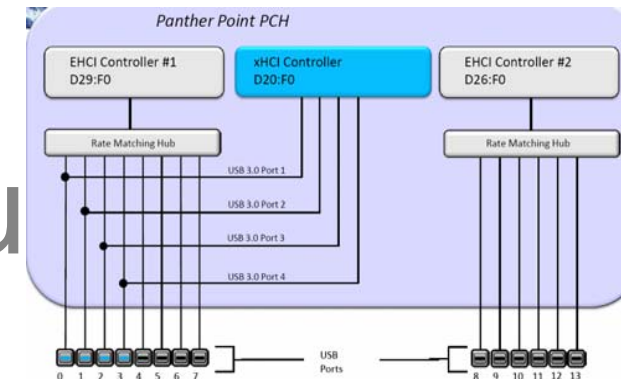
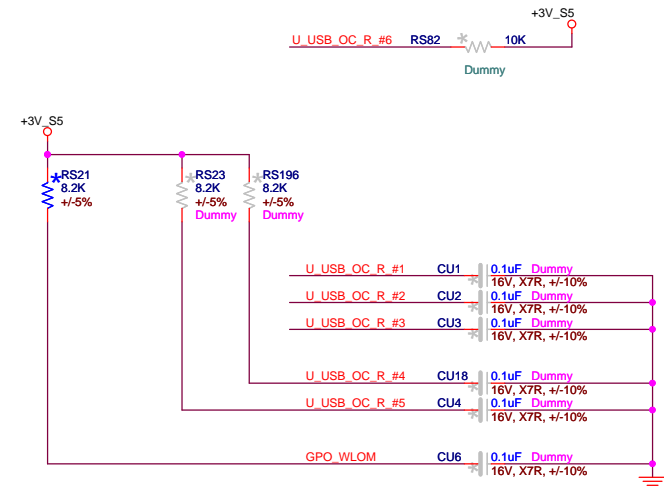
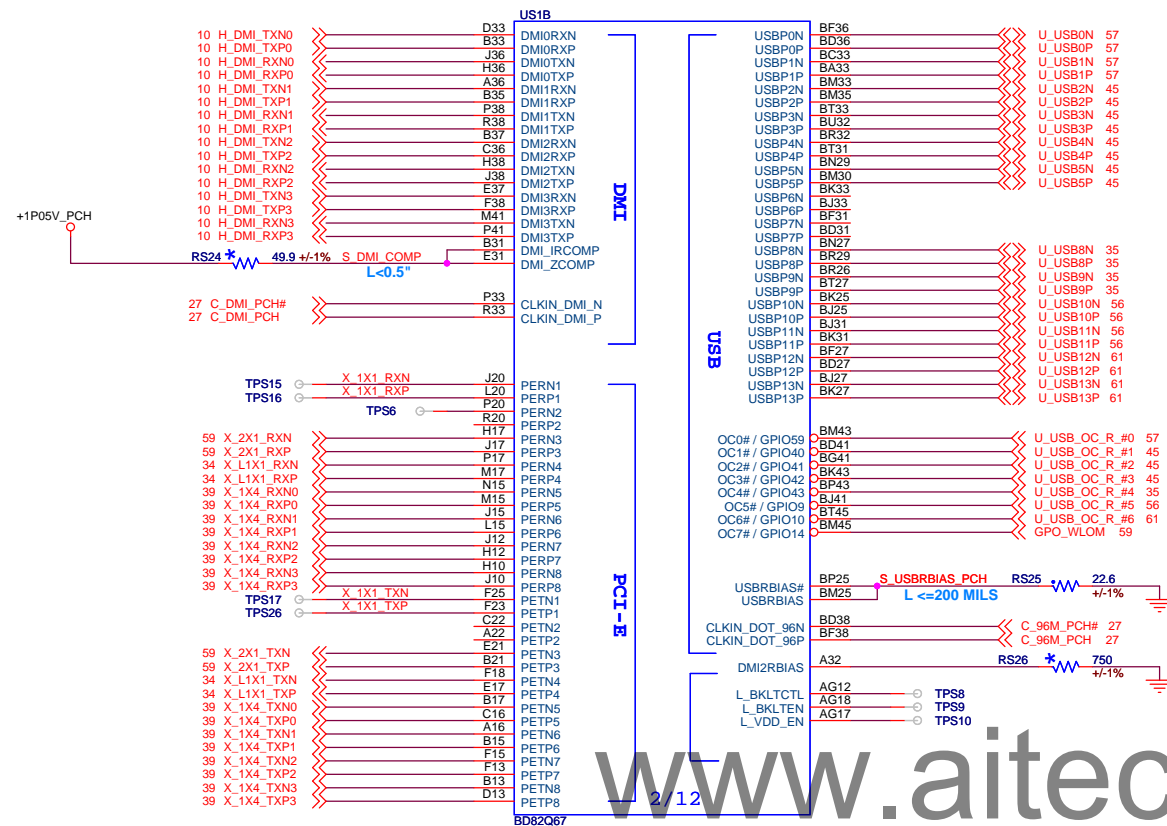
GNT2#/GPIO53:ESI strap for server platform
ONLY,Do not pull low.



Title
PCH-1: PCI

DWG NO
Lanikai MT/DT

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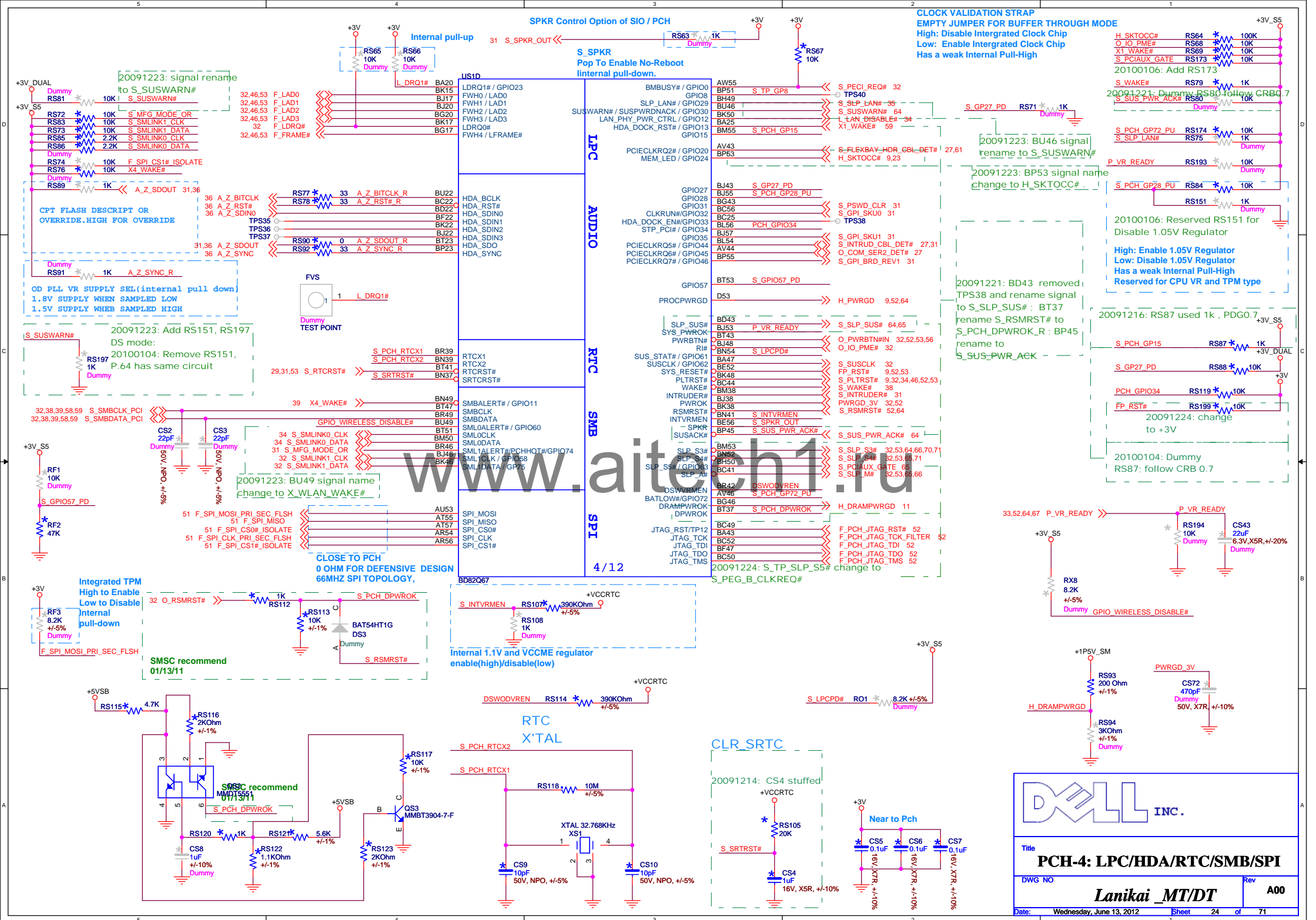
| USB2.0 | USB3.0 | Lainikai OC Pin | Power | Function | Standard OC pin configuration |
|---------------------------------|-------------------|-----------------|---------------|--------------|-------------------------------|
| Port 0 U_USB0N U_USB0P | USB3.0 Port 1 | U_USB_OC_R_#0 | USBPWR1_F_50 | Front USB3.0 | OC0# |
| Port 1 U_USB1N U_USB1P | USB3.0 Port 2 | U_USB_OC_R_#1 | USBPWR2_F_50 | Rear USB3.0 | OC1# |
| Port 2 U_USB2N U_USB2P | USB3.0 Port 3 | U_USB_OC_R_#2 | USBPWR4_F_50 | Rear USB2.0 | OC2# |
| Port 3 U_USB3N U_USB3P | USB3.0 Port 4 | U_USB_OC_R_#3 | USBPWR5_F_50 | Rear USB2.0 | OC2# |
| Port 4 U_USB4N U_USB4P | USB3.0 Port 5 | U_USB_OC_R_#4 | USBPWR6_F_50 | Rear USB2.0 | OC4# |
| Port 5 U_USB5N U_USB5P | USB3.0 Port 6 | U_USB_OC_R_#5 | USBPWR7_F_50 | Front USB2.0 | OC5# |
| Port 6 U_USB6N U_USB6P | USB3.0 Port 7 | U_USB_OC_R_#6 | USBPWR8_F_50 | INT_USB | OC6# |
| Port 7 U_USB7N U_USB7P | USB3.0 Port 8 | U_USB_OC_R_#7 | USBPWR9_F_50 | INT_USB | OC6# |
| Port 8 U_USB8N U_USB8P | USB3.0 Port 9 | U_USB_OC_R_#8 | USBPWR10_F_50 | INT_USB | OC6# |
| Port 9 U_USB9N U_USB9P | USB3.0 Port 10 | U_USB_OC_R_#9 | USBPWR11_F_50 | INT_USB | OC6# |
| Port 10 U_USB10N U_USB10P | USB3.0 Port 11 | U_USB_OC_R_#10 | USBPWR12_F_50 | INT_USB | OC6# |
| Port 11 U_USB11N U_USB11P | USB3.0 Port 12 | U_USB_OC_R_#11 | USBPWR13_F_50 | INT_USB | OC6# |
| Port 12 U_USB12N U_USB12P | USB3.0 Port 13 | U_USB_OC_R_#12 | USBPWR14_F_50 | INT_USB | OC6# |
| Port 13 U_USB13N U_USB13P | USB3.0 Port 14 | U_USB_OC_R_#13 | USBPWR15_F_50 | INT_USB | OC6# |

Intel

PCH-2: DMI/PCIe/USB

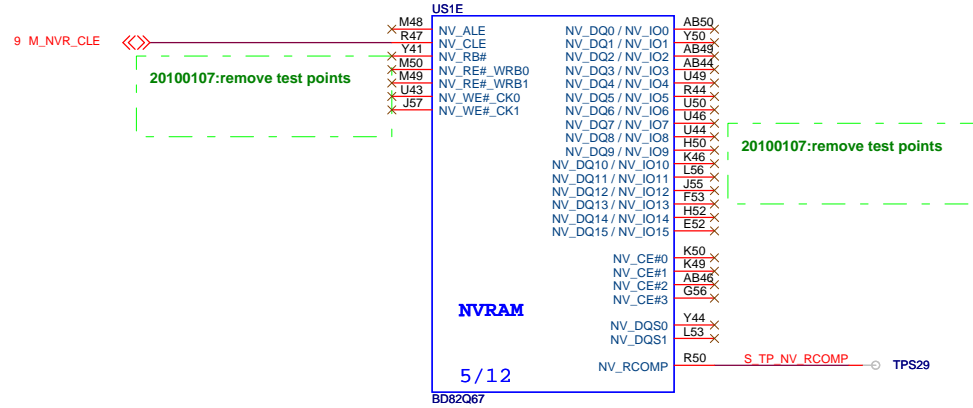
DWG NO **Lanikai_MT/DT** Rev **A00**

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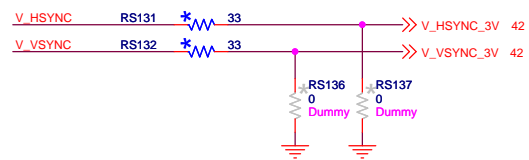
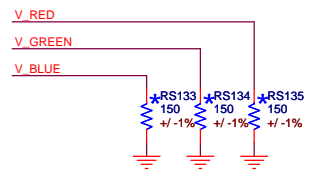
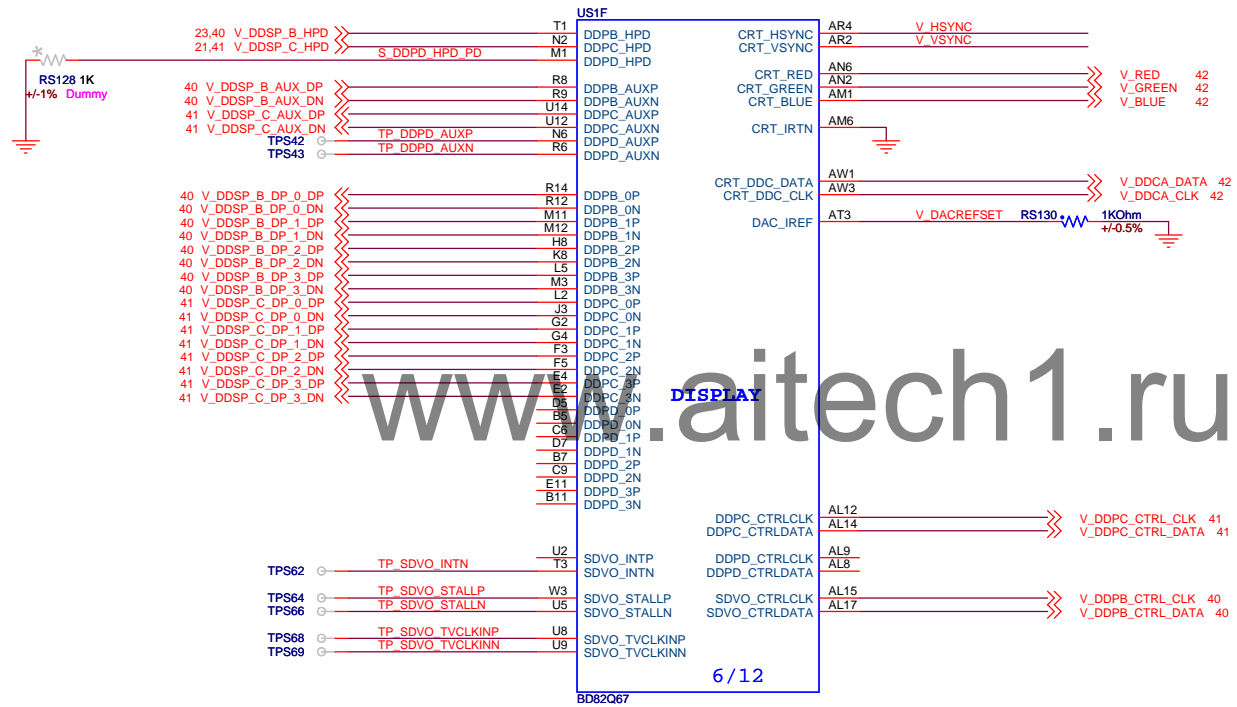



20100106: Remove ONFI function since not support

S_NVR_CLE internal pull-down.



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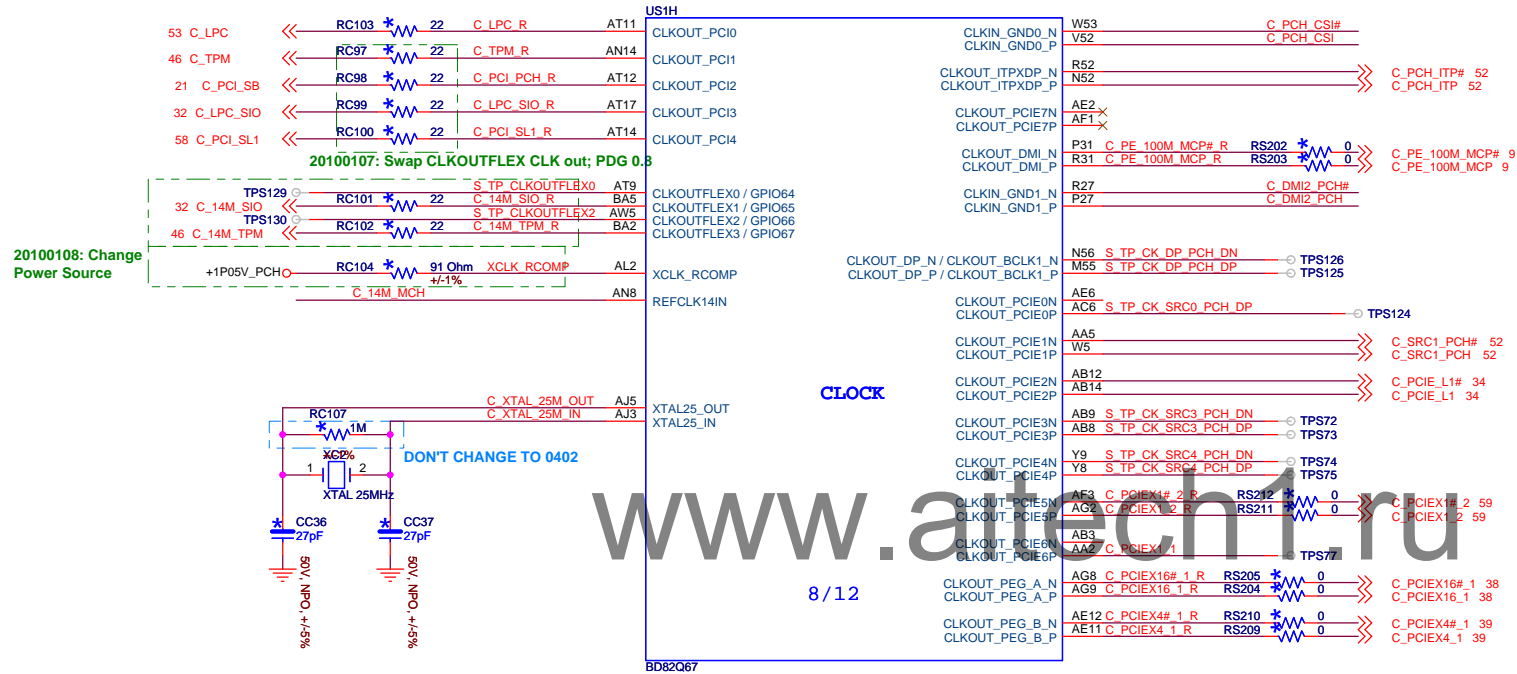


Title
PCH-6: Display

DWG NO **Lanikai_MT/DT** Rev **A00**

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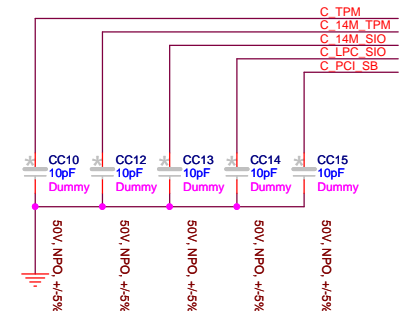
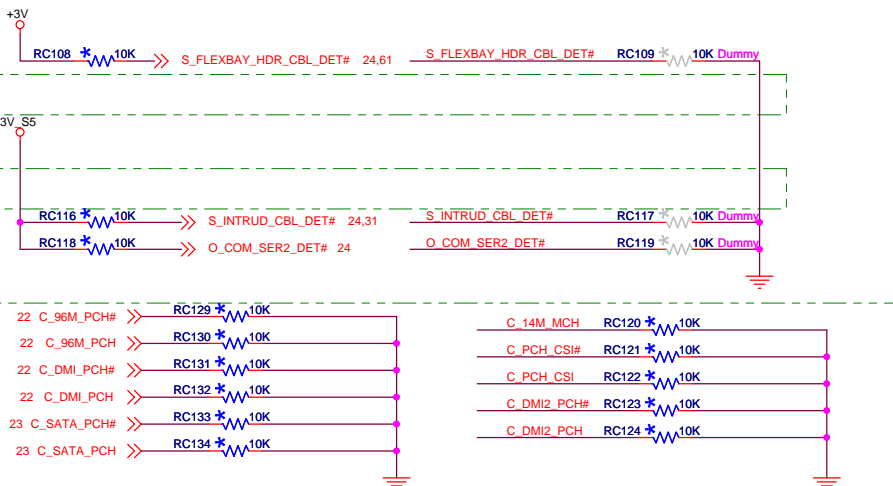
20100106: Remove RS96; CRB 0.7
20100106: Swap C_PCH_PCIE0_R and C_PCH_PCIE1_R; CRB 0.7
20100106: Disconnect AT11 and left Test point; CRB 0.7



20091216 PCIECLKRQ1#/GPIO18 is mobile chip only, RC110, RC111 and signal net "S_PCIECLKREQ#1" removed.

20100106: GPO_WLOM move to GPIO14

Pull-down for Integrated clock gen-11/25/09
20100105: Dummy all pull-down resistors since use buffer thru mode
20100106: Reserved RC123,RC124; CRB 0.7
20100107: RC121,RC122 mount; PDG 0.8



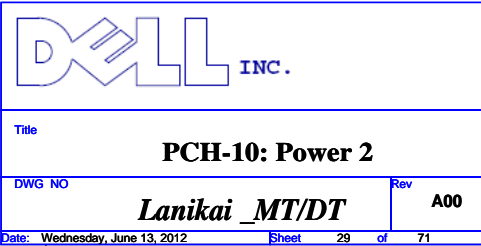
PCH-8: Clock

DWG NO

Lanikai MT/DT

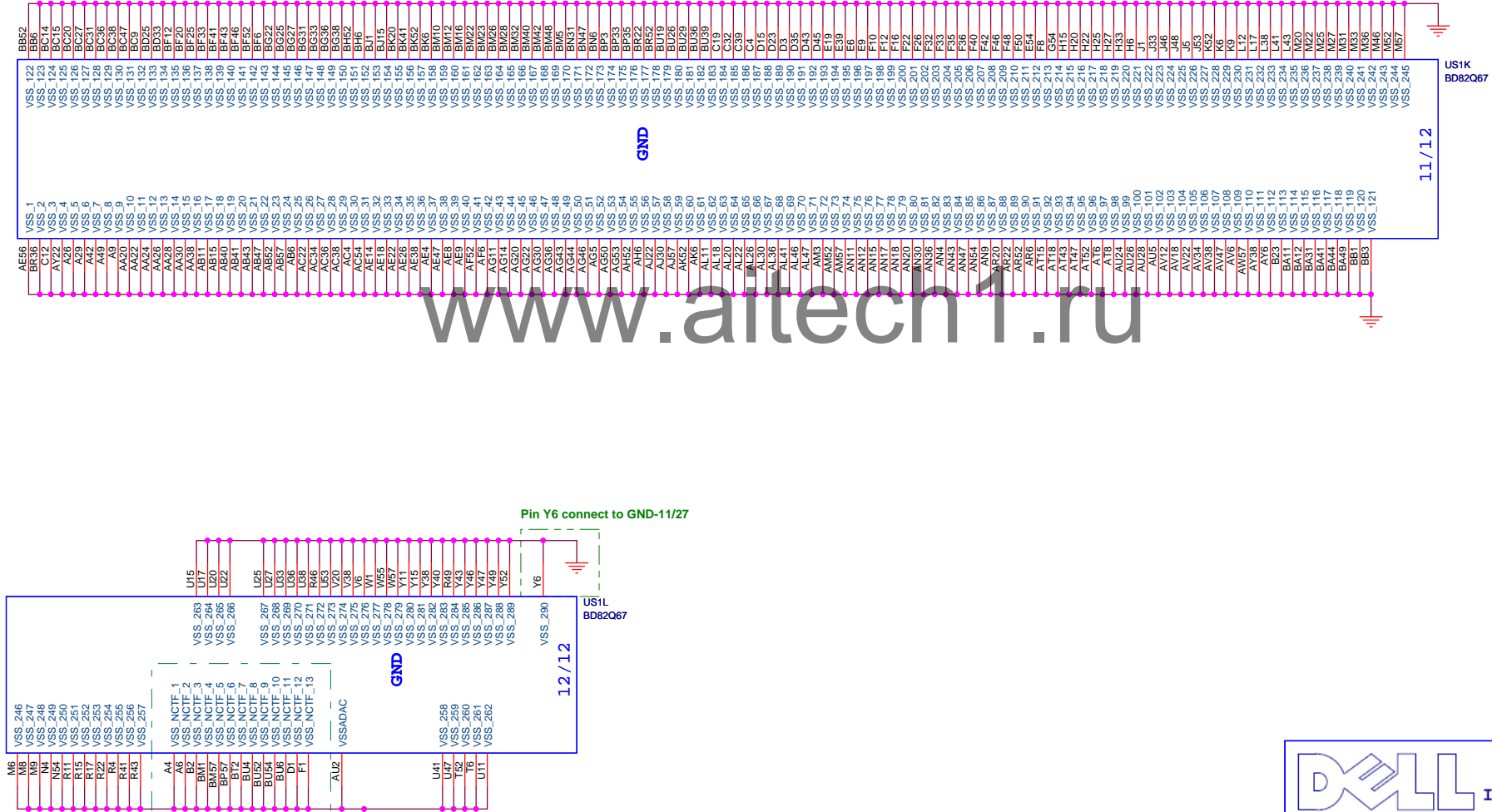
Rev A00

Date: Wednesday, June 13, 2012 Sheet 27 of 71

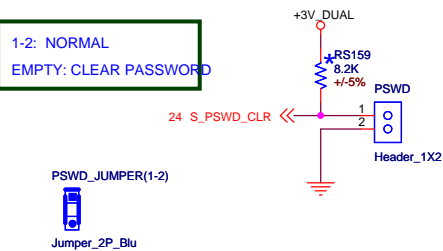


2011_1115

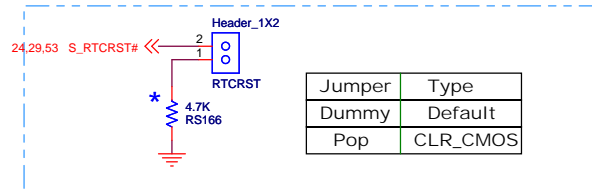
By Dell request remove US1_1 PCH heatsink detect for RTCSRST net spacing



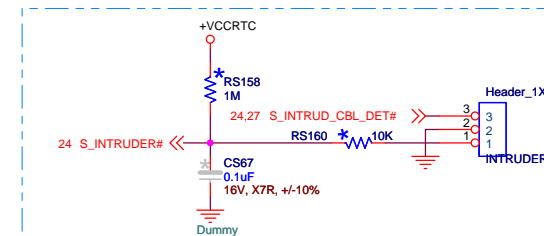
Clear Password



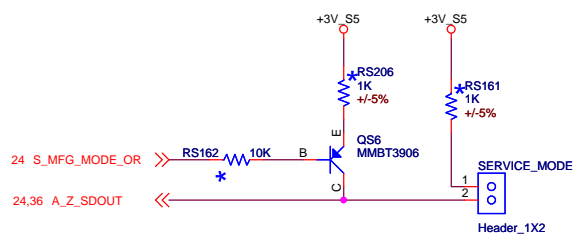
CLR_CMOS



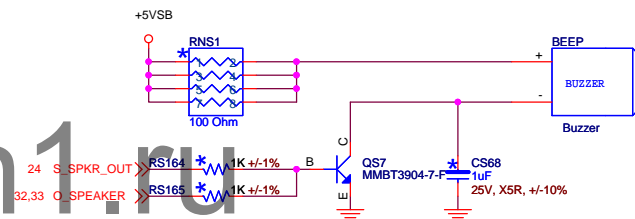
Chassis Intruder



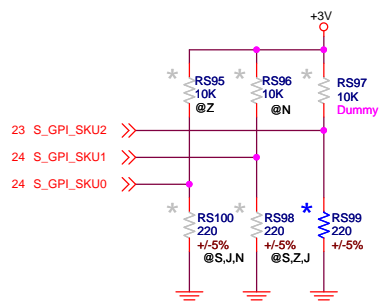
SERVICE_MODE



BEEP



SKU ID



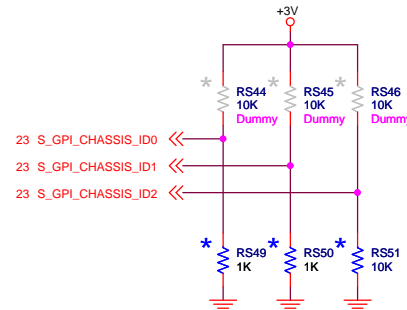
SKU ID

| SKU1 | SKU0 | Type |
|------|------|-------------|
| 0 | 0 | TPM |
| 0 | 1 | TCM |
| 1 | 0 | non TPM/TCM |
| 1 | 1 | Reserved |

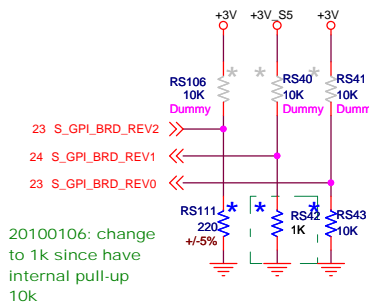
Chassis ID

check : need to update table

| ID2 | ID1 | ID0 | Type |
|-----|-----|-----|---------|
| 1 | 0 | 1 | SFF |
| 1 | 0 | 0 | Comoros |
| 0 | 0 | 0 | MT/DT |
| 0 | 1 | 1 | USFF |



BOARD ID



| Rev2 | Rev1 | Rev0 | Type |
|------|------|------|----------|
| 0 | 0 | 0 | Default |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |



Delet RO2; SMSC suggestion-12/08/09

Delet RO6; SMSC suggestion-12/08/09

20100107: change to +3V_DUAL for layout

Delet RO33,RO34; SMSC suggestion-12/08/09

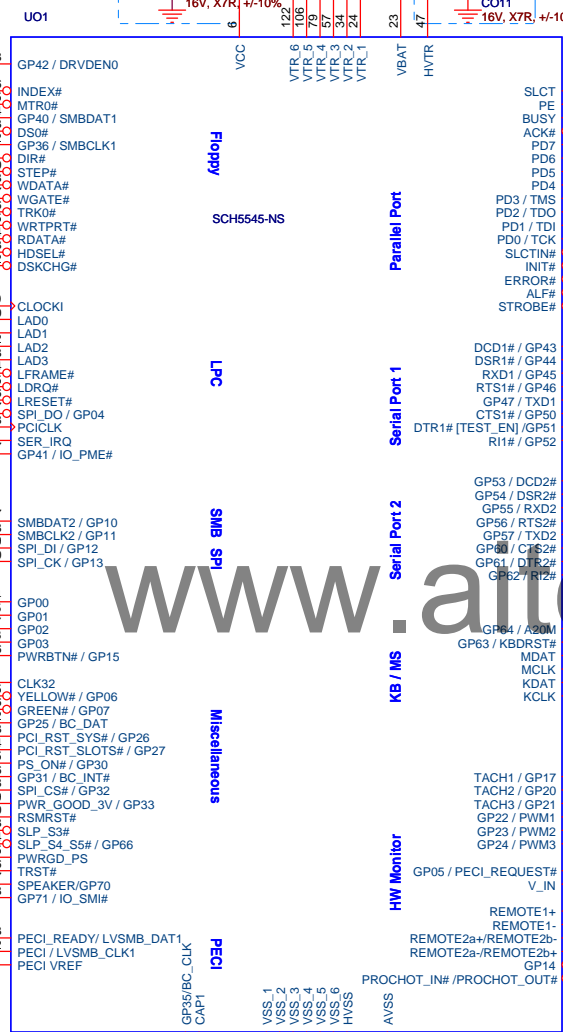
Net change to H_RESET#-12/28/09

Reserved RO35; SMSC suggestion-12/08/09

20100111: Remove PSU PWM control

DO1 change to RO109; SMSC suggestion-12/08/09

Delet RO36,RO37 and connect Tmin_Shift to PCH directly; SMSC suggestion-12/08/09



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Title

SIO-SCH5544-1

DWG NO

Lanikai MT/DT

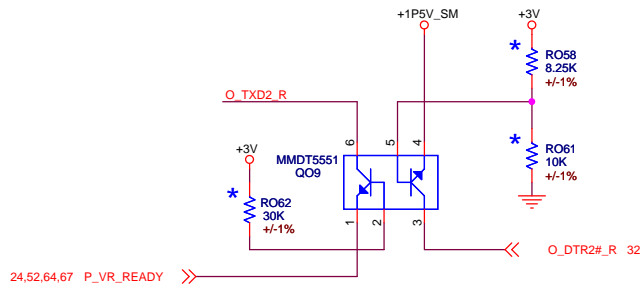
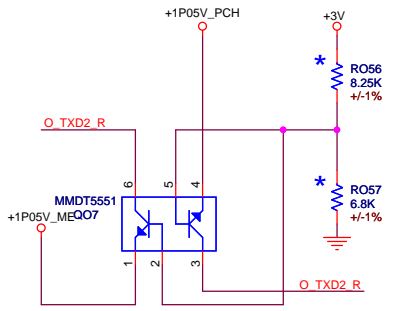
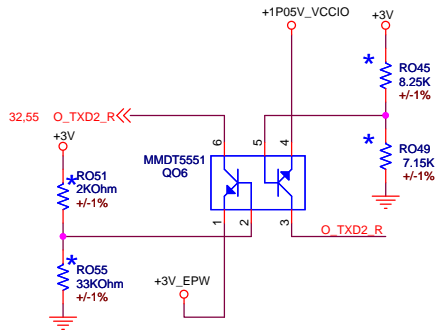
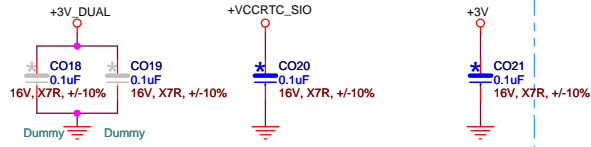
Rev

A00

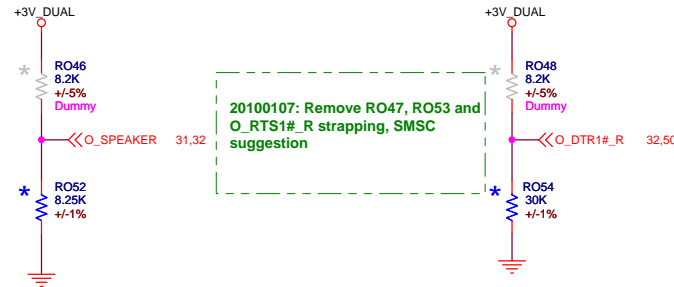
Date: Wednesday, June 13, 2012

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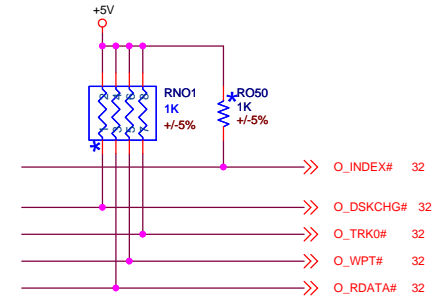
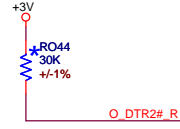
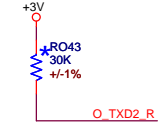
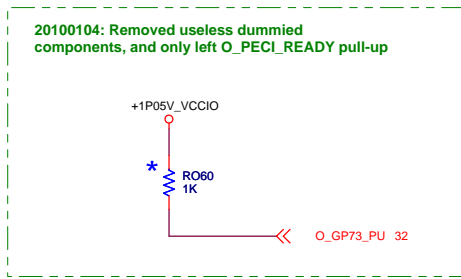
SCH5544 Decoupling



5544 PRE-POST DIAG PG GENERATION

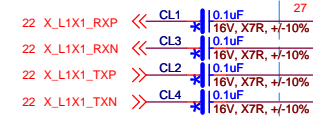


| | SPEAKER | DTR1# |
|-----------|---------|-----------------|
| | Diag_En | Flash_en |
| PULL HIGH | Disable | Flash Enable |
| PULL LOW | Enable | Parallel Enable |



20091216 Intel 82579 schematic check list 0.5:
Change net name from CLK_REQ_N to S_FLEXBAY_HDR_CBL_DET#
20100105: Remove RL2 and S_FLEXBAY_HDR_CBL_DET#
connection since useless; PDG 0.8

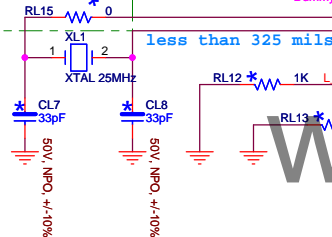
near the PCIe transmitter.



24 S_SMLINK0_CLK
24 S_SMLINK0_DATA

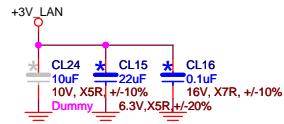
L LAN_DISABLE#

20091216 CRB0.7 :Connect a series CL24
(10 pF) capacitor to XTAL_OUT (pin 9)!



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Close to PIN5 (VDD)



20091216 follow CRB0.7 and 82579 checklist: does not require
any MDI termination.(delete => RL15, RL16, RL17, RL18, RL19,
RL20, RL21, RL22, CL11, CL12, CL13, CL14)



Title

LAN: Intel Lewisvillies

DWG NO

Lanikai MT/DT

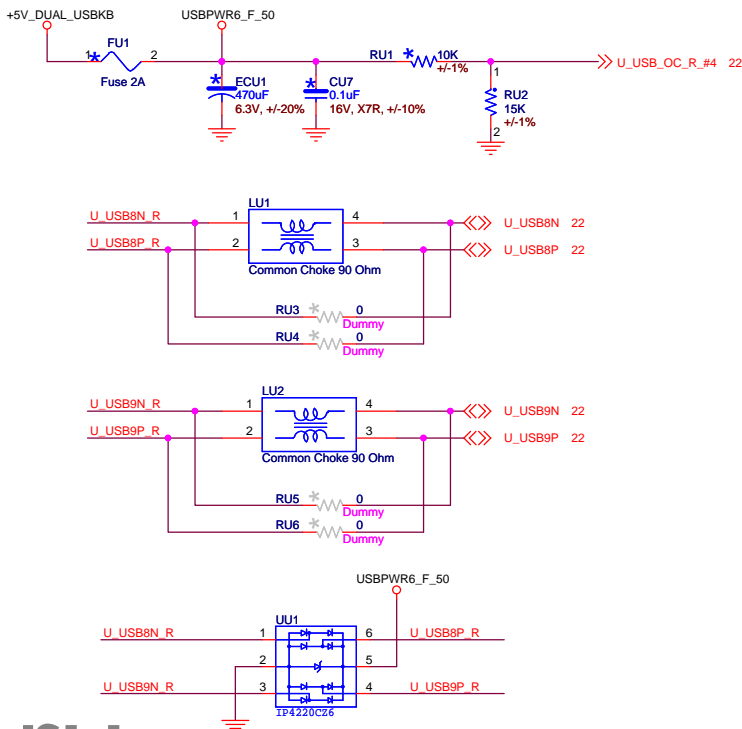
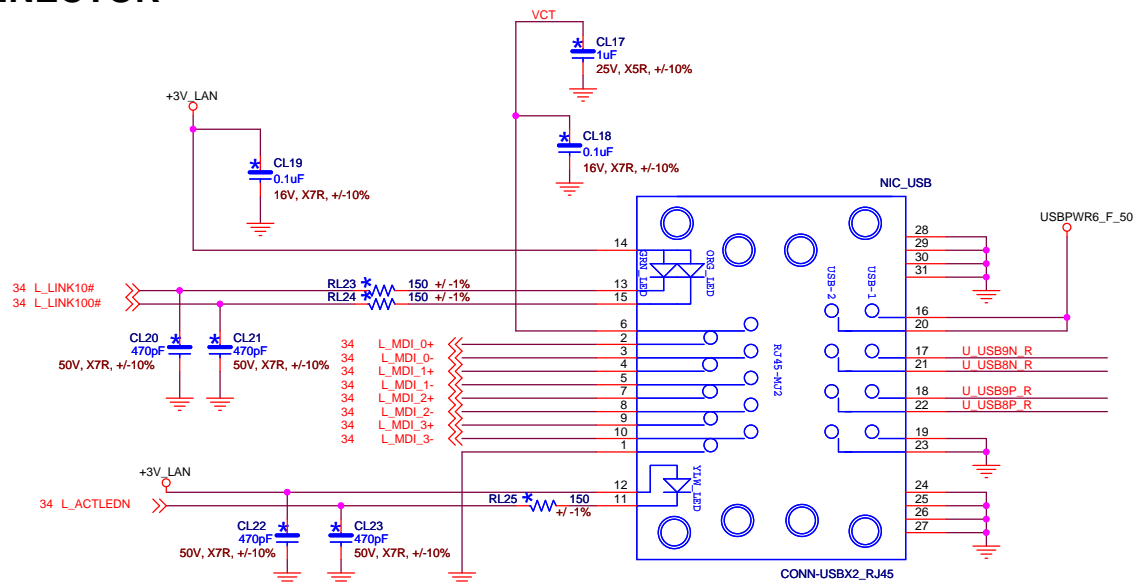
Rev

A00

Date: Wednesday, June 13, 2012

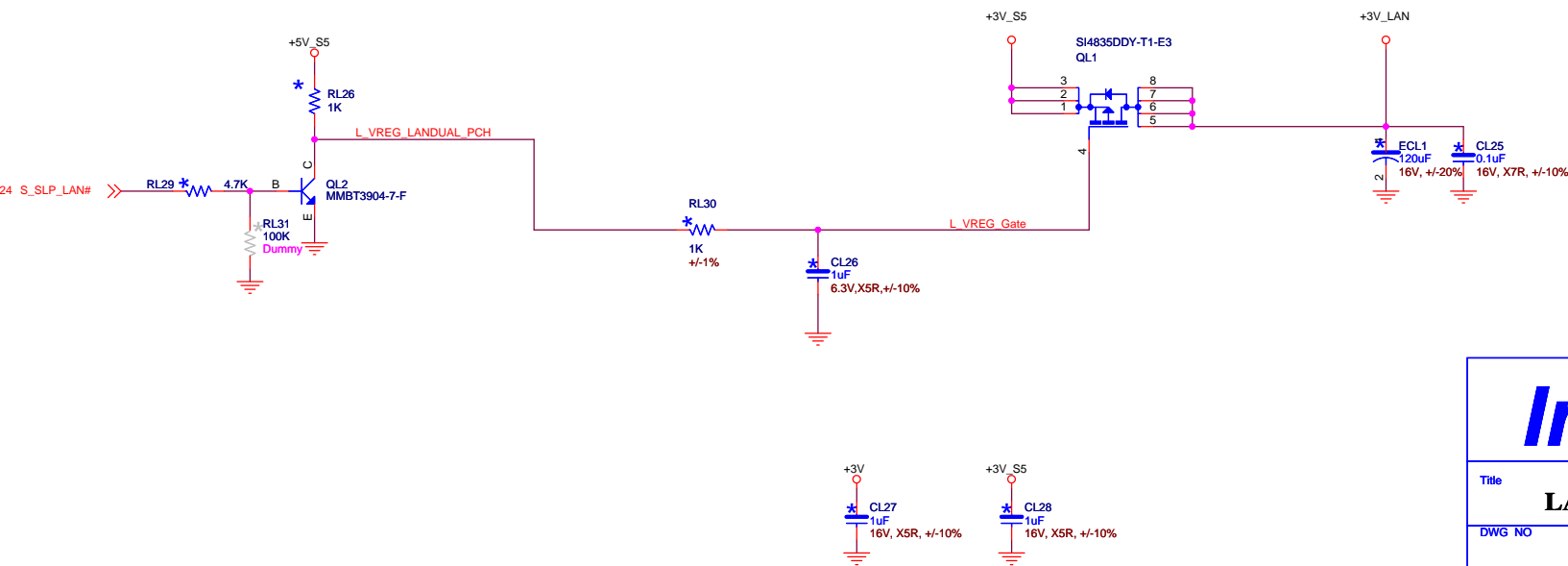
Sheet 34 of 71


LAN CONNECTOR



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LAN POWER





Intel

Title

LAN Power & LAN/USB Conn

DWG NO

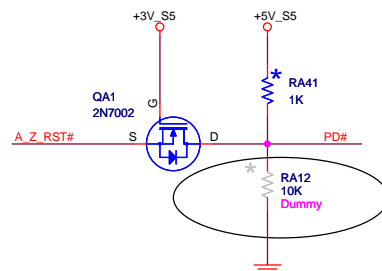
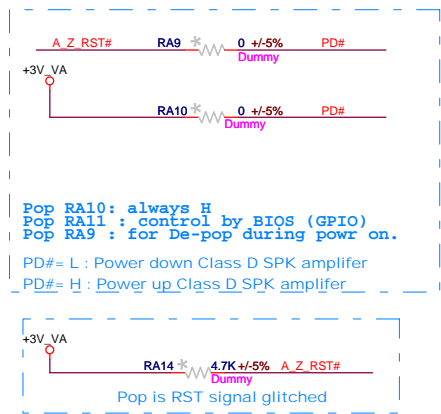
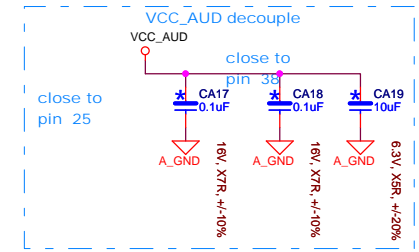
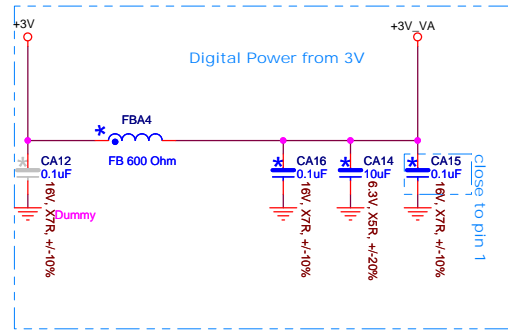
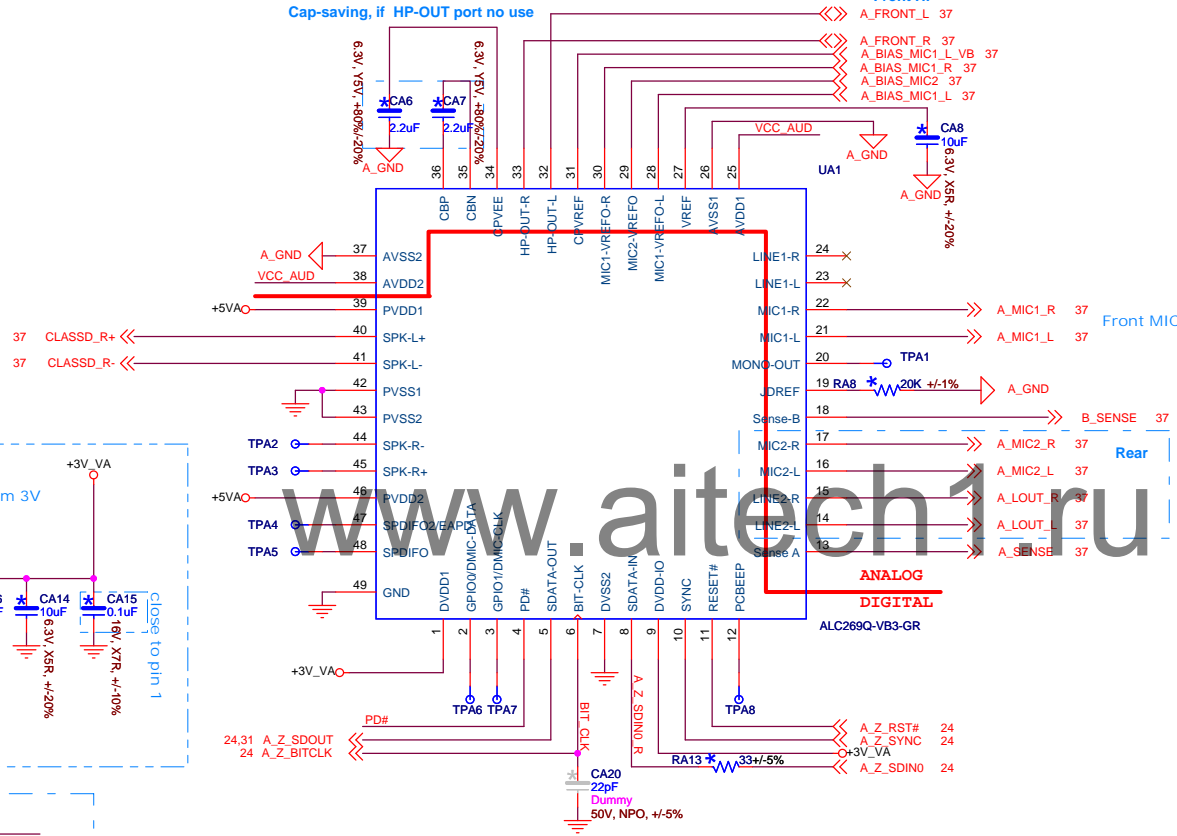
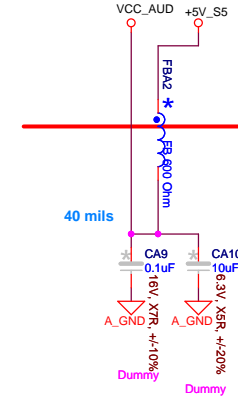
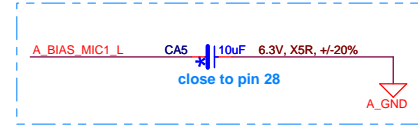
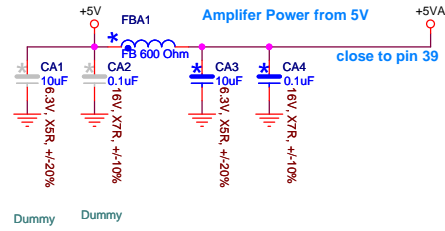
Lanikai_MT/DT

Rev

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10 X_1X16_TXP[15..0] >>
10 X_1X16_TXN[15..0] >>

24,32,39,58,59 S_SMBCLK_PCI
24,32,39,58,59 S_SMBDATA_PCI

RX1 0 Dummy
RX2 0 Dummy

24 S_WAKE# <<

X_1X16_TXP0 CX36
X_1X16_TXN0 CX37

220nF 16V,X7R,+/-10% X_EXP A TX_C DP0
220nF 16V,X7R,+/-10% X_EXP A TX_C DN0

X_1X16_TXP1 CX34
X_1X16_TXN1 CX35

220nF 16V,X7R,+/-10% X_EXP A TX_C DP1
220nF 16V,X7R,+/-10% X_EXP A TX_C DN1

X_1X16_TXP2 CX32
X_1X16_TXN2 CX33

220nF 16V,X7R,+/-10% X_EXP A TX_C DP2
220nF 16V,X7R,+/-10% X_EXP A TX_C DN2

X_1X16_TXP3 CX30
X_1X16_TXN3 CX31

220nF 16V,X7R,+/-10% X_EXP A TX_C DP3
220nF 16V,X7R,+/-10% X_EXP A TX_C DN3

X_1X16_TXP4 CX28
X_1X16_TXN4 CX29

220nF 16V,X7R,+/-10% X_EXP A TX_C DP4
220nF 16V,X7R,+/-10% X_EXP A TX_C DN4

X_1X16_TXP5 CX26
X_1X16_TXN5 CX27

220nF 16V,X7R,+/-10% X_EXP A TX_C DP5
220nF 16V,X7R,+/-10% X_EXP A TX_C DN5

X_1X16_TXP6 CX24
X_1X16_TXN6 CX25

220nF 16V,X7R,+/-10% X_EXP A TX_C DP6
220nF 16V,X7R,+/-10% X_EXP A TX_C DN6

X_1X16_TXP7 CX22
X_1X16_TXN7 CX23

220nF 16V,X7R,+/-10% X_EXP A TX_C DP7
220nF 16V,X7R,+/-10% X_EXP A TX_C DN7

X_1X16_TXP8 CX20
X_1X16_TXN8 CX21

220nF 16V,X7R,+/-10% X_EXP A TX_C DP8
220nF 16V,X7R,+/-10% X_EXP A TX_C DN8

X_1X16_TXP9 CX18
X_1X16_TXN9 CX19

220nF 16V,X7R,+/-10% X_EXP A TX_C DP9
220nF 16V,X7R,+/-10% X_EXP A TX_C DN9

X_1X16_TXP10 CX15
X_1X16_TXN10 CX17

220nF 16V,X7R,+/-10% X_EXP A TX_C DP10
220nF 16V,X7R,+/-10% X_EXP A TX_C DN10

X_1X16_TXP11 CX13
X_1X16_TXN11 CX14

220nF 16V,X7R,+/-10% X_EXP A TX_C DP11
220nF 16V,X7R,+/-10% X_EXP A TX_C DN11

X_1X16_TXP12 CX11
X_1X16_TXN12 CX12

220nF 16V,X7R,+/-10% X_EXP A TX_C DP12
220nF 16V,X7R,+/-10% X_EXP A TX_C DN12

X_1X16_TXP13 CX7
X_1X16_TXN13 CX10

220nF 16V,X7R,+/-10% X_EXP A TX_C DP13
220nF 16V,X7R,+/-10% X_EXP A TX_C DN13

X_1X16_TXP14 CX5
X_1X16_TXN14 CX6

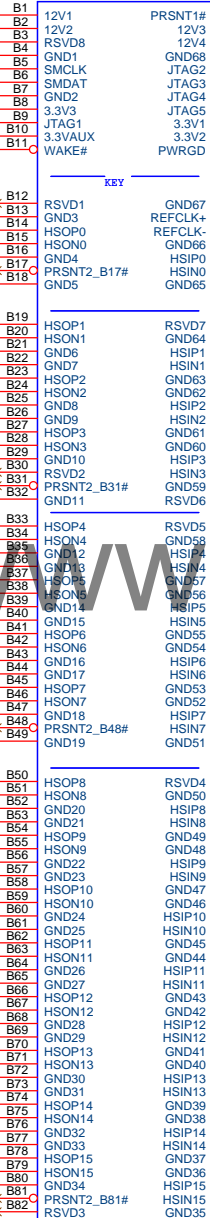
220nF 16V,X7R,+/-10% X_EXP A TX_C DP14
220nF 16V,X7R,+/-10% X_EXP A TX_C DN14

X_1X16_TXP15 CX3
X_1X16_TXN15 CX4

220nF 16V,X7R,+/-10% X_EXP A TX_C DP15
220nF 16V,X7R,+/-10% X_EXP A TX_C DN15

2010317: Slot1 change to Blue,
Foxconn P/N: 34030EK00-600-G

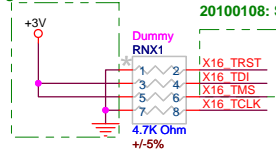
SLOT1



Slot-PCIE-16X

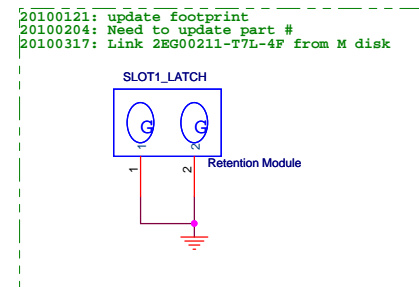
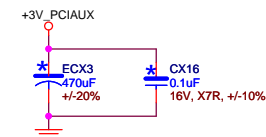
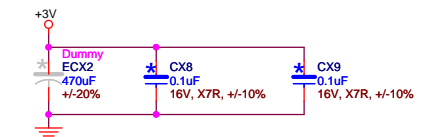
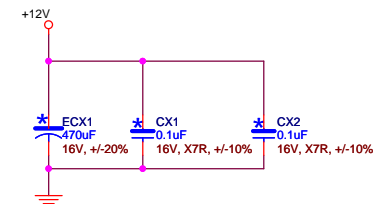
340303U00-600-G
340304R00-278-G
340304J00-317-G
340306Y00-GRS-G

20100513: RNX1 pin1 change
connection to GND and pin5
change connection to +3V



20100108: Swap pin for layout

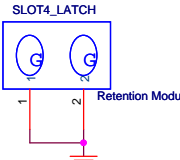
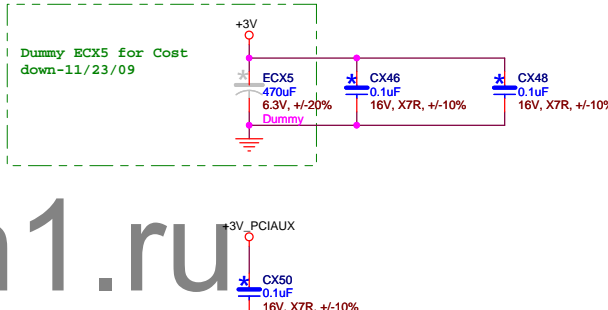
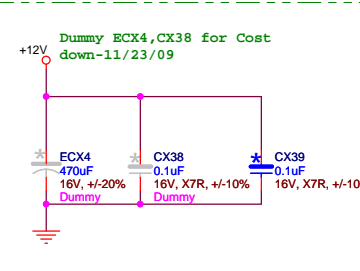
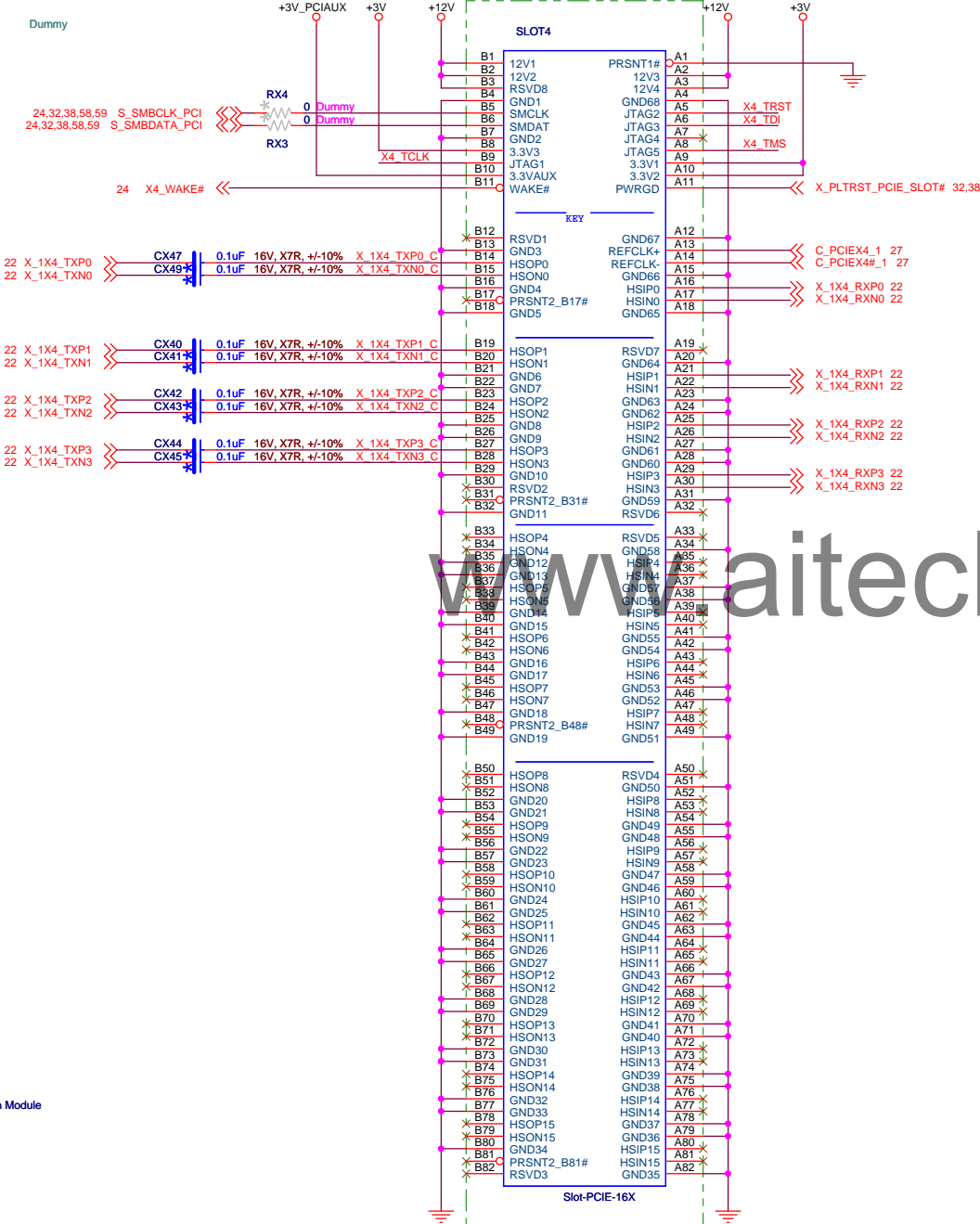
>>> X_1X16_RXP[15..0] 10
>>> X_1X16_RXN[15..0] 10



20100121: update footprint
20100204: Need to update part #
20100317: Link 2BG00211-T7L-4F from M disk



| | | | |
|--------------------------------|--|-----------------|----------|
| Title | | Slot1: PCIe 16x | |
| DWG NO | | Rev | A00 |
| Date: Wednesday, June 13, 2012 | | Sheet | 38 of 71 |

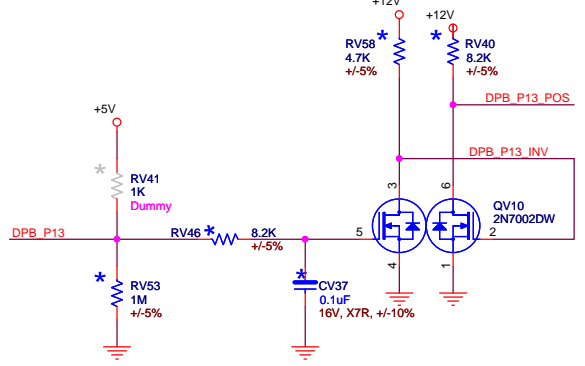
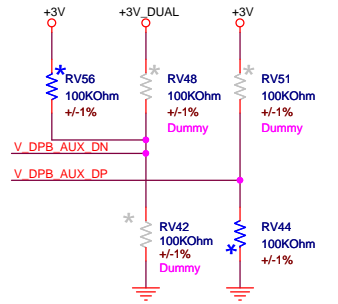
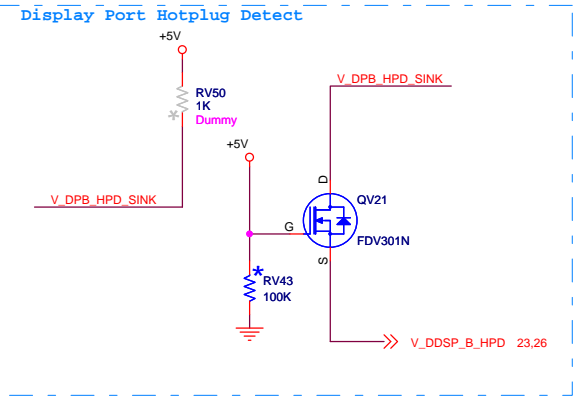
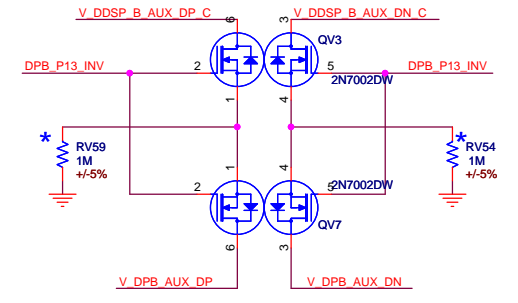
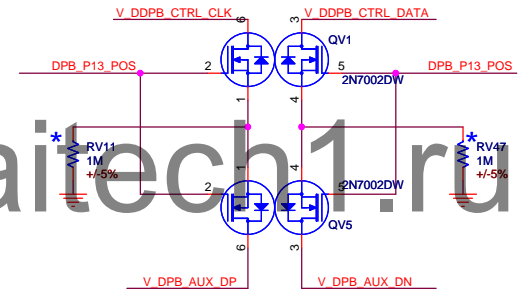
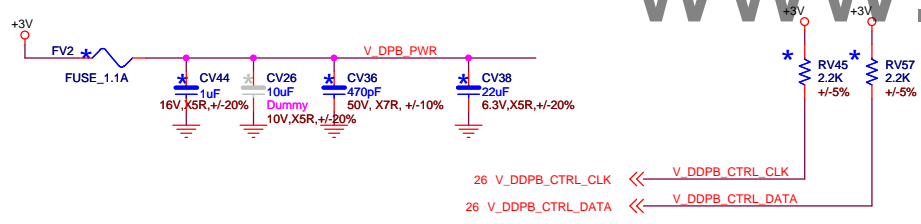
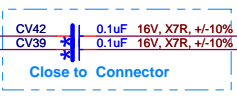
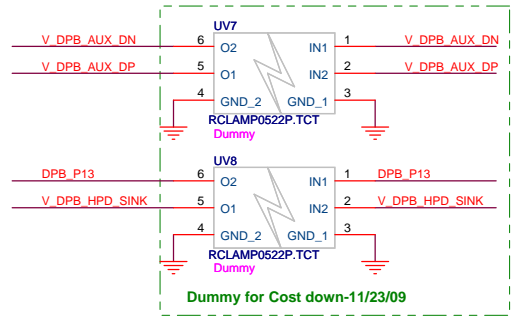
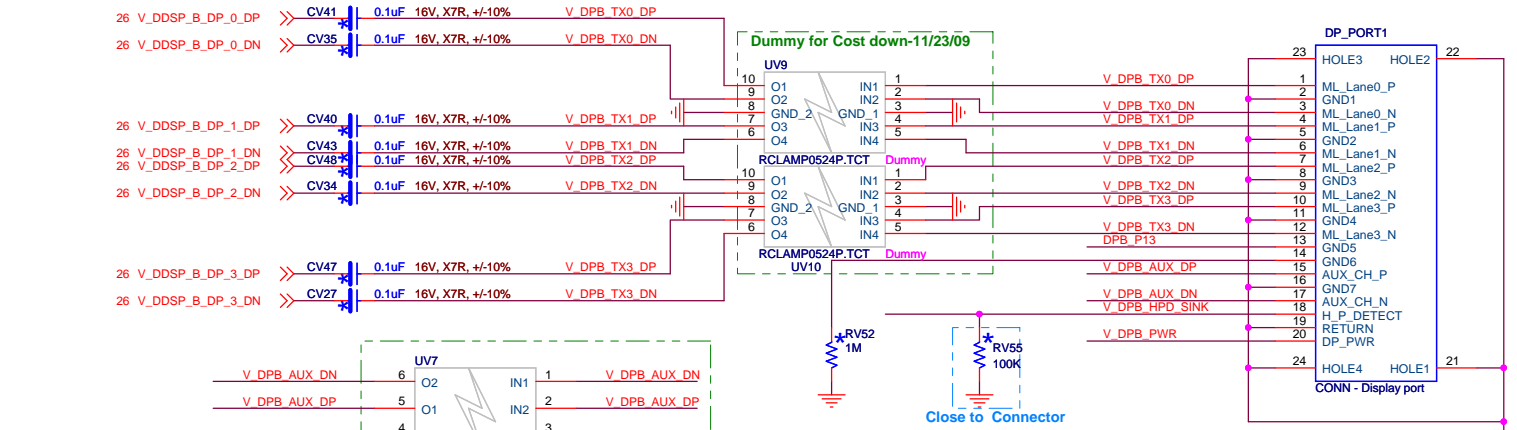
**Slot4: PCIe 4x**

DWG No.

Lanikai MT/DT

| | |
|-----|-----|
| Rev | A00 |
|-----|-----|

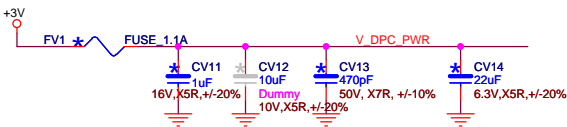
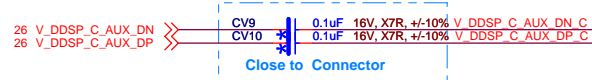
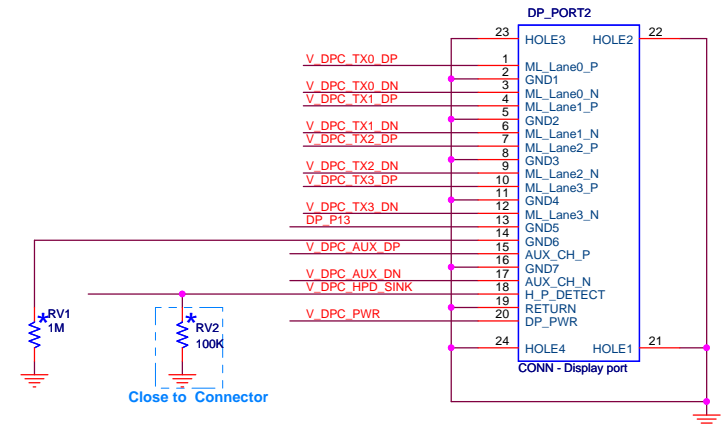
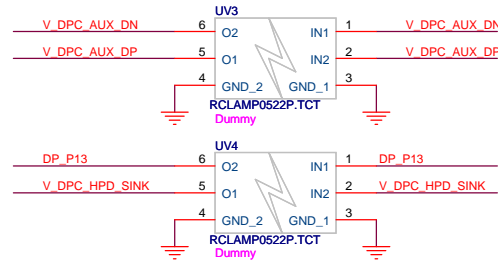
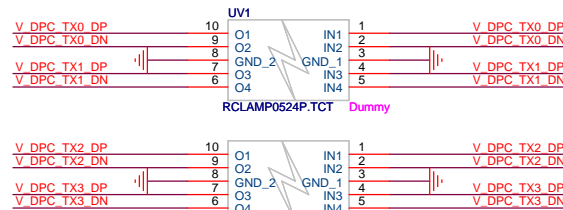
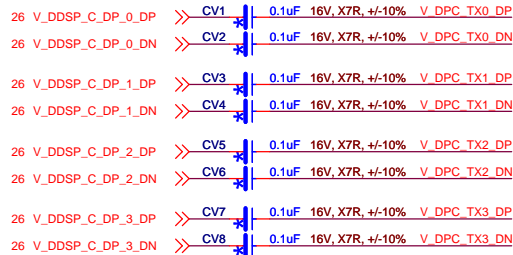
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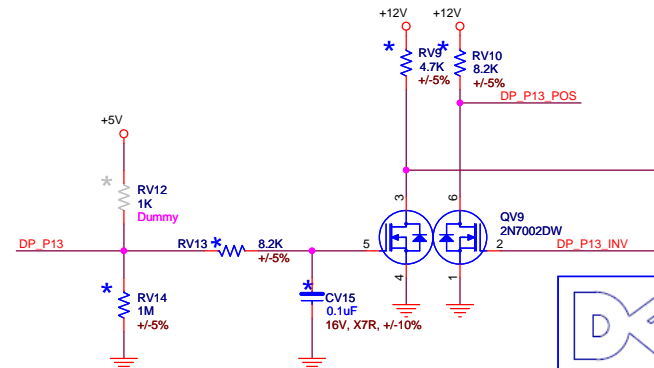
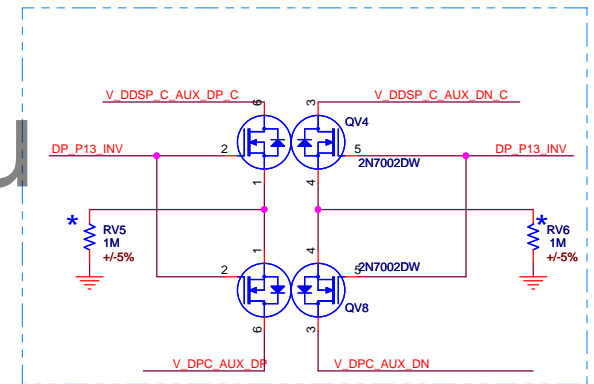
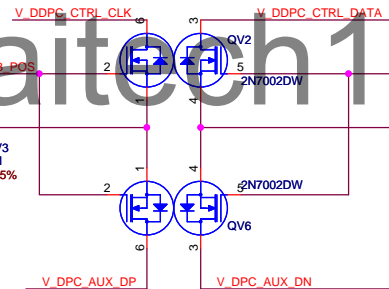
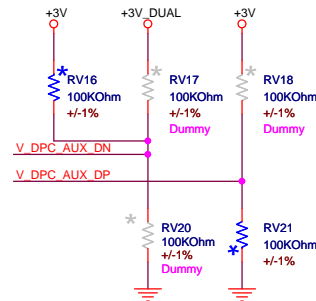
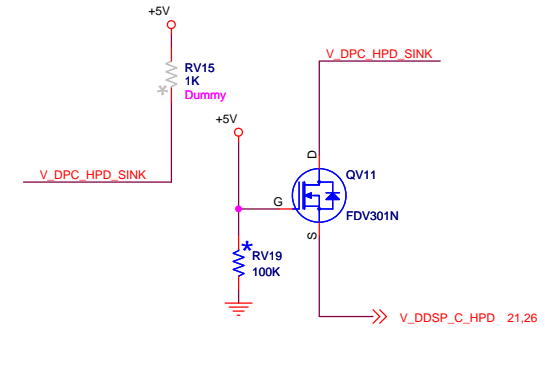
DVI-D+VGA Conn

DWG NO **Lanikai_MT/DT** Rev **A00**

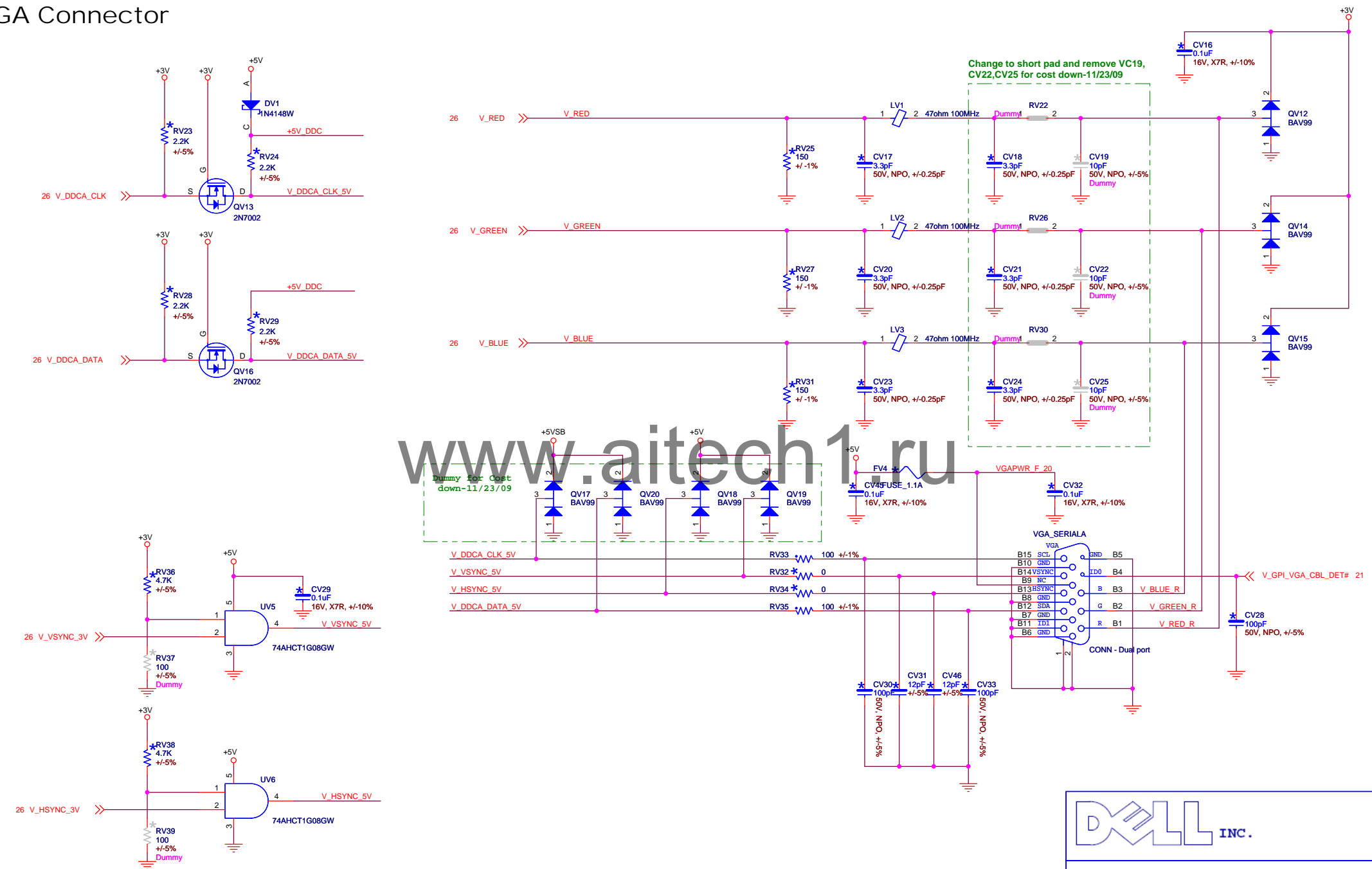
Date: Wednesday, June 13, 2012 Sheet 40 of 71




Display Port Hotplug Detect



VGA Connector



 **INC.**

Title

VGA Conn

DWG NO

Lanikai MT/DT

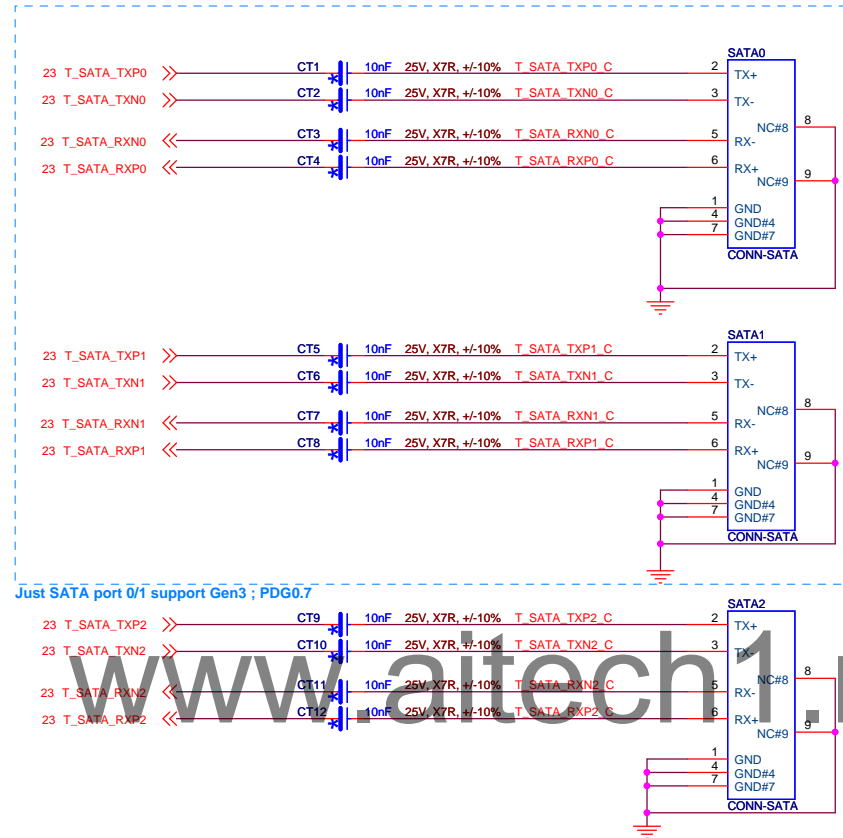
Rev

A00

Date: Wednesday, June 13, 2012


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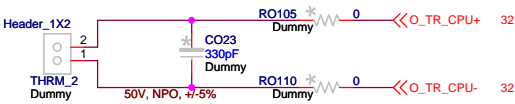
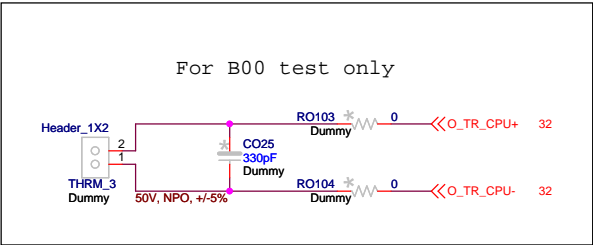
SATA x 3



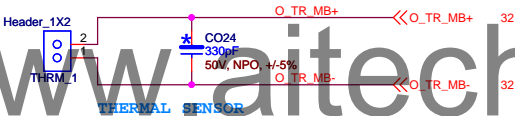
| | |
|--|--------------------------|
| | |
| Title SATA Conn | |
| DWG NO Lanikai_MT/DT | Rev A00 |
| Date: Wednesday, June 13, 2012 Sheet 43 of 71 | |

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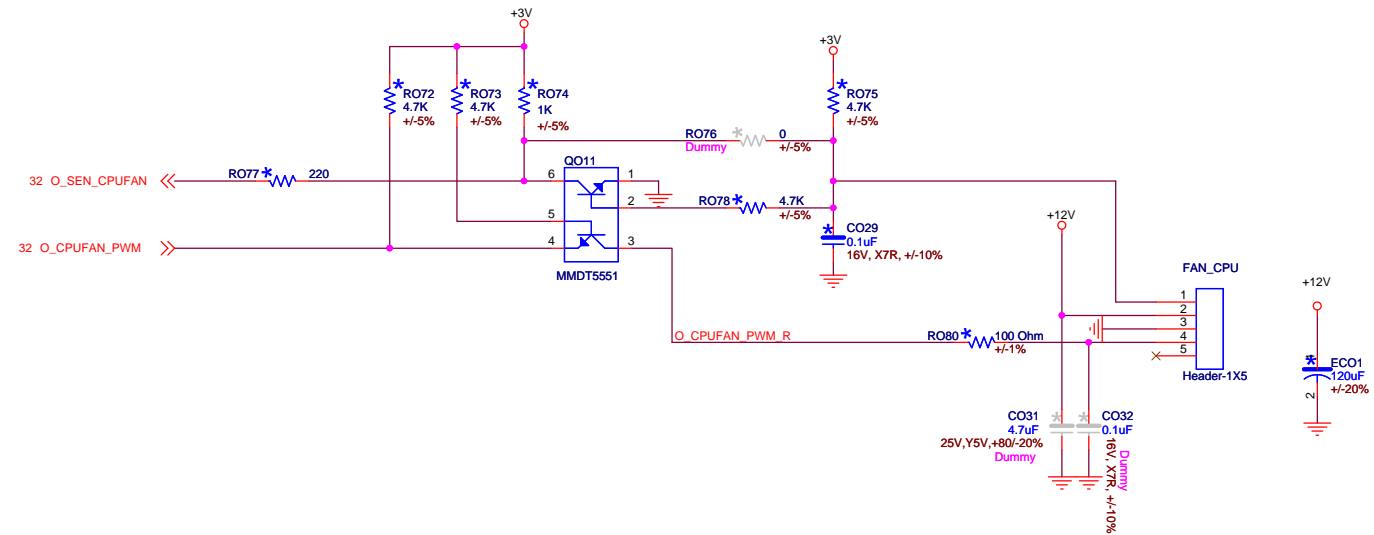
| | | |
|---|-----------------------------|-------------------|
|  | | |
| Title TBD | | |
| DWG NO | <i>Lanikai_MT/DT</i> | Rev A00 |
| Date: Wednesday, June 13, 2012 | Sheet 44 of 71 | |



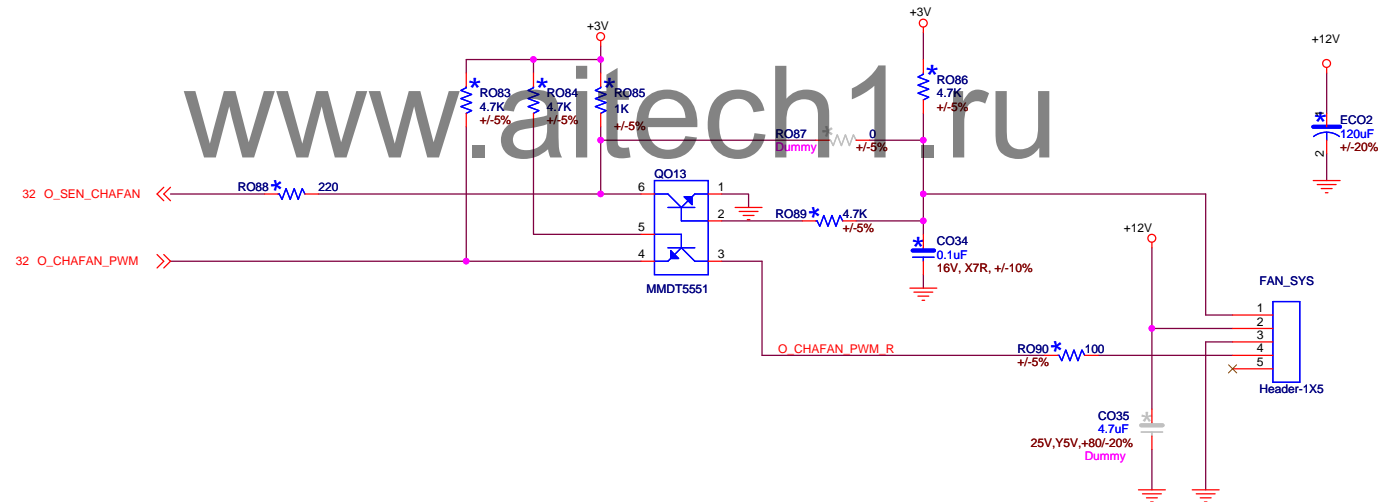
Dummy THRM2,CO23; ME suggestion-12/04/09



CPU Fan



SYS Fan



Title

FAN

| | |
|--------|--|
| DWG NO | |
|--------|--|

Lanikai_MT/DT

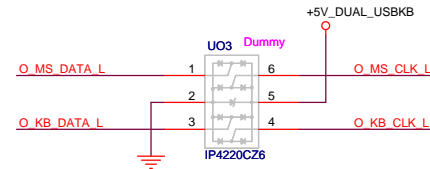
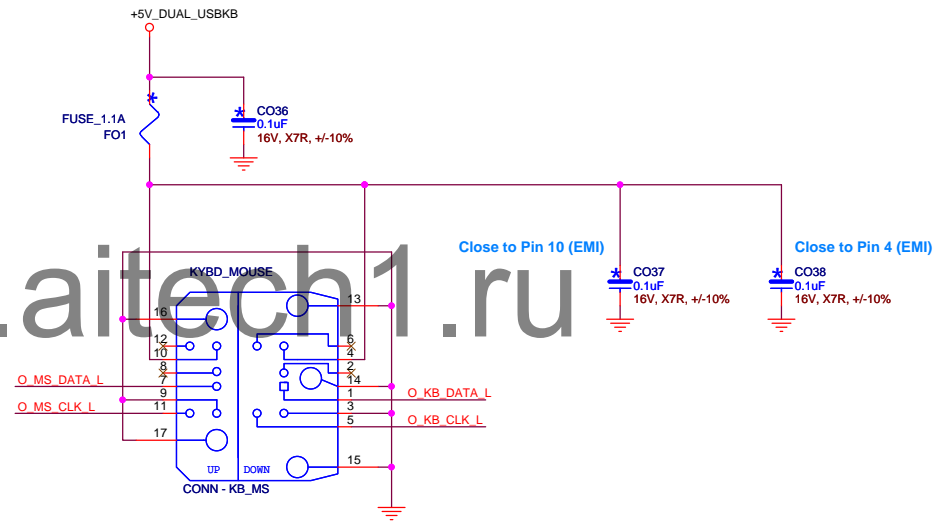
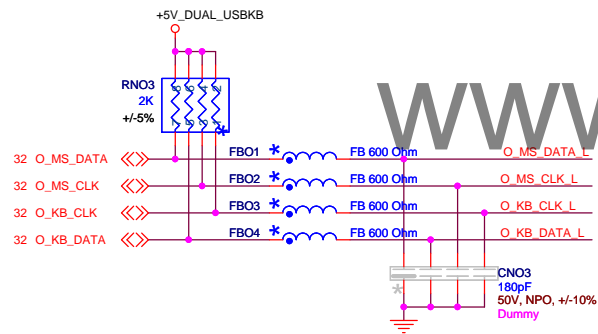
Rev


A00

Date: Wednesday, June 13, 2012

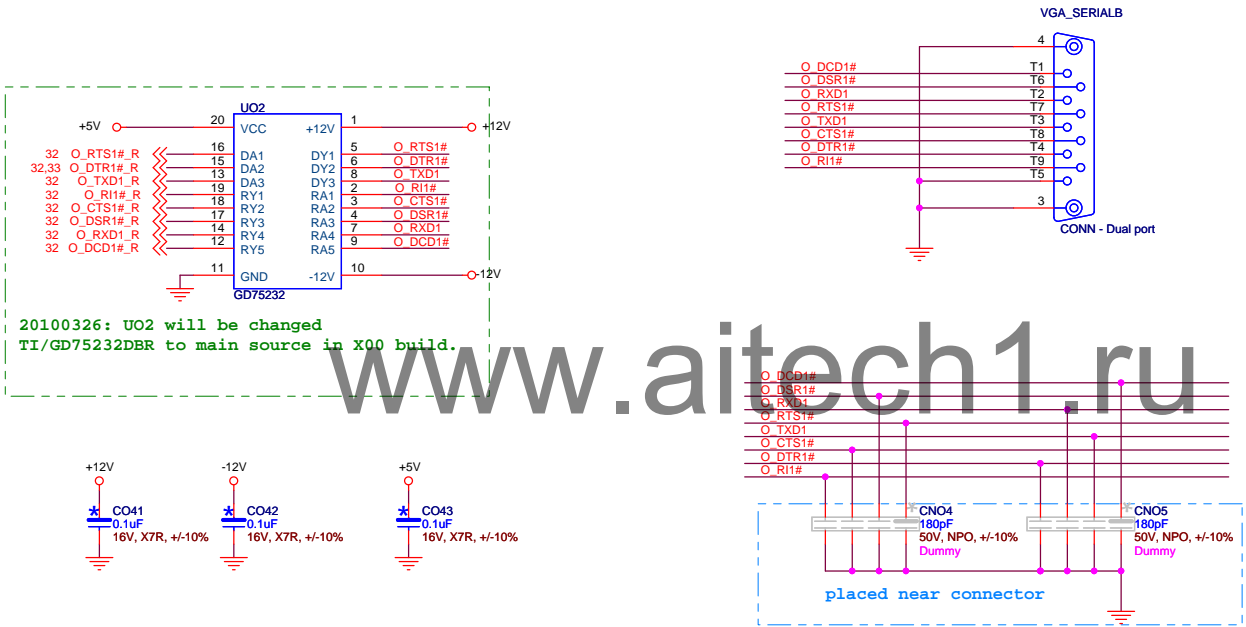
Sheet 48 of 71

KB/MS

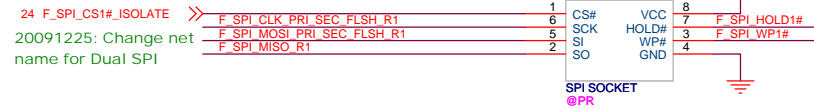


| | |
|---|----------------|
|  | |
| Title | |
| PS2 Conn | |
| DWG NO | Rev |
| Lanikai_MT/DT | A00 |
| Date: Wednesday, June 13, 2012 | Sheet 49 of 71 |

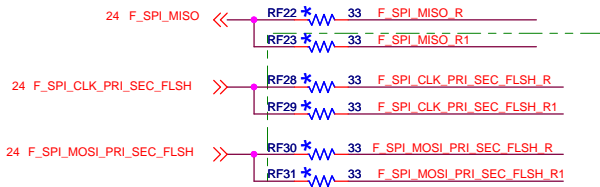
Serial Port 1



SPI



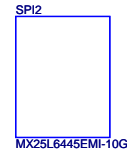
20110530: Change to 4M



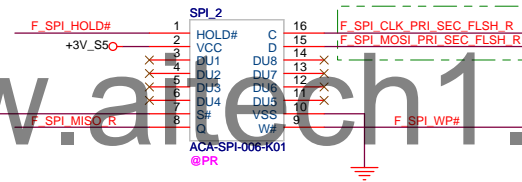
20091225: RF23 change to 33ohm for Dual SPI
20091225: Add RF28, RF29, RF30, RF31 for Dual SPI

24 F_SPI_CS0#_ISOLATE >>

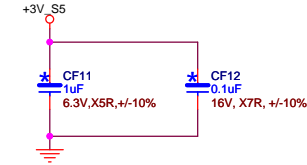
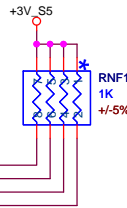
20100309: SPI2 Package Type change to DIP from SMD, when usage SPI_2 socket
20100930: SPI2 change to MXIC_MX25L6445EMI-10G



20091225: Change net name for Dual SPI



20091225: Change net name for Dual SPI



Title

SPI

DWG NO

Lanikai_MT/DT

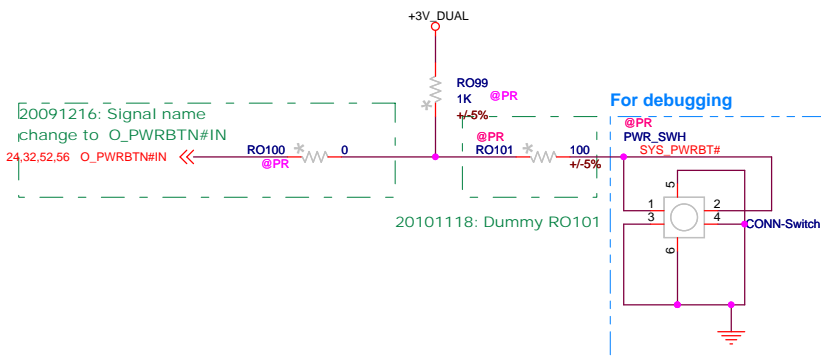
Rev

A00

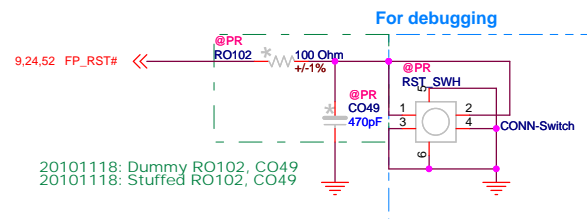
Date: Wednesday, June 13, 2012

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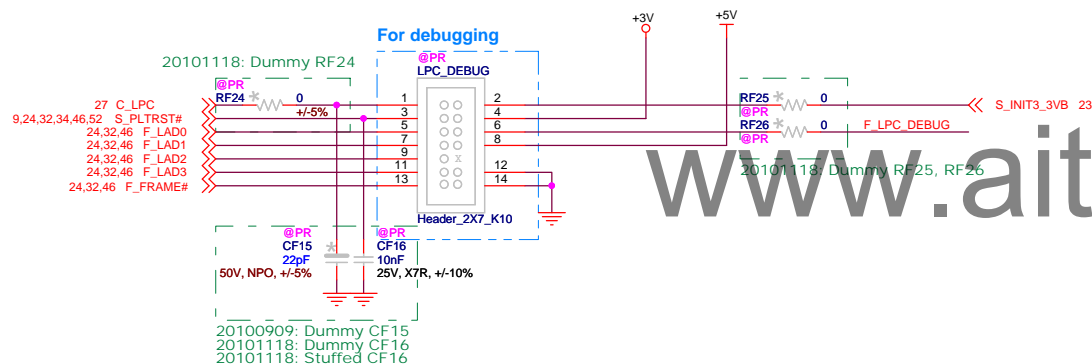
Power Bottom



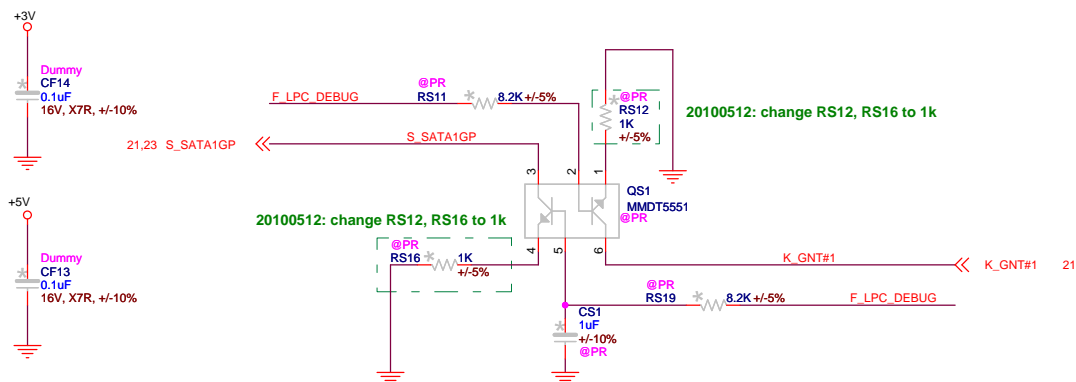
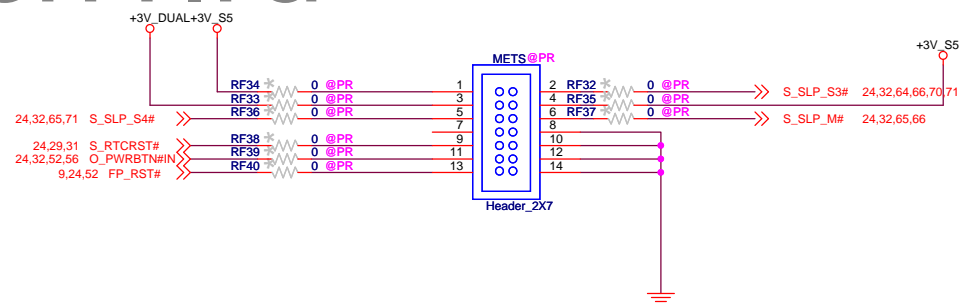
Reset Bottom



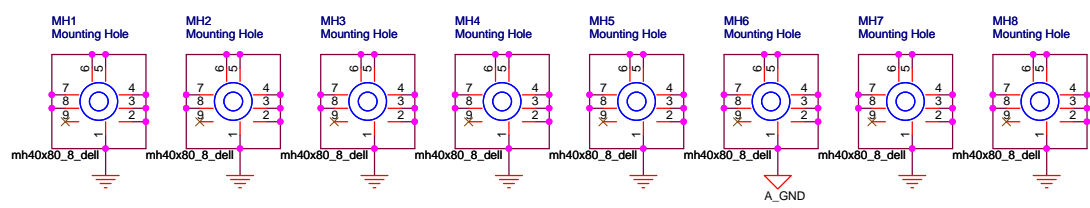
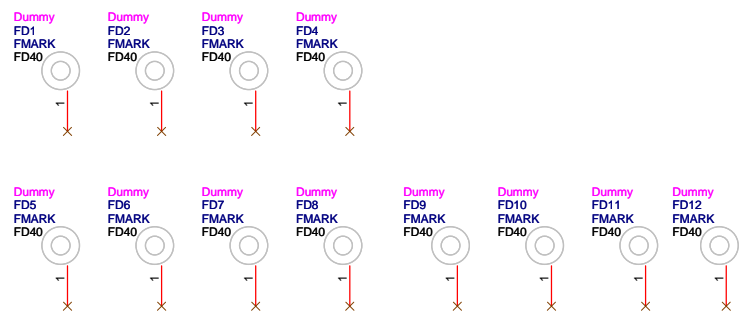
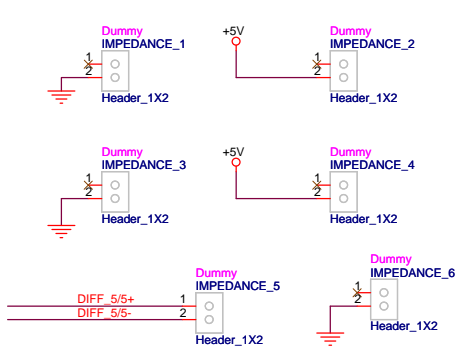
LPC DEBUG



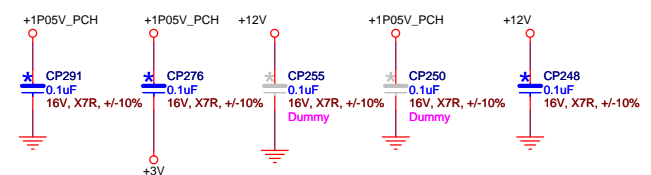
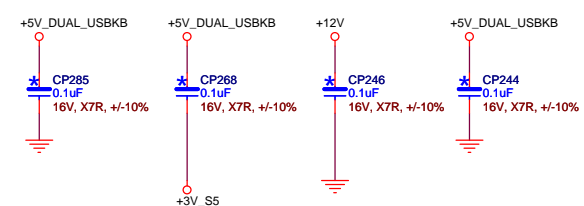
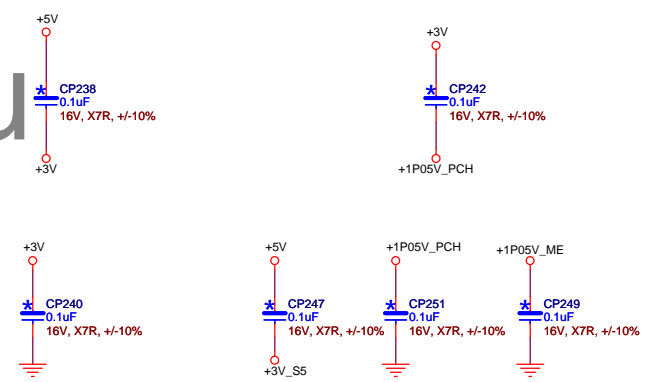
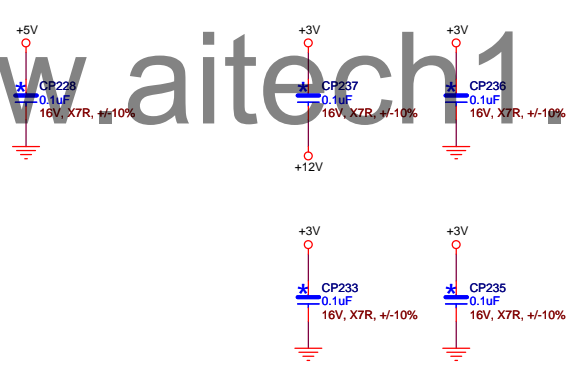
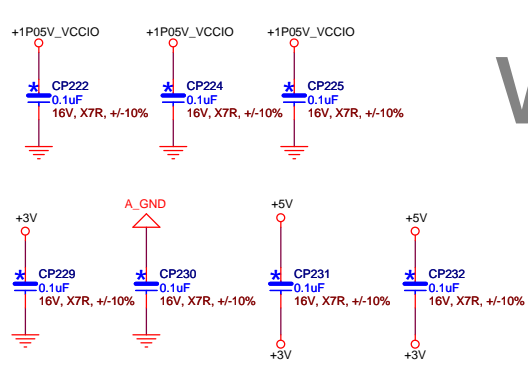
APS Connector




| | | | |
|-----------------------|--------------------------|------------|----------|
| | | | |
| Pilot Run Conn | | | |
| DWG NO | Lanikai_MT/DT | | Rev |
| | | A00 | |
| Date: | Wednesday, June 13, 2012 | Sheet | 53 of 71 |



20100108: Add for EMI

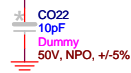
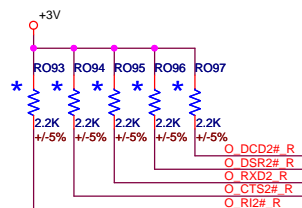




| | | |
|------------|--------------------------|----------------|
| EMI | | |
| DWG NO | Lanikai MT/DT | Rev |
| | | A00 |
| Date: | Wednesday, June 13, 2012 | Sheet 54 of 71 |

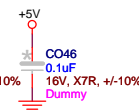
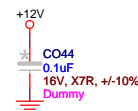
Move PWR_SW conn to
page56 20091126

Serial Port 2 Header



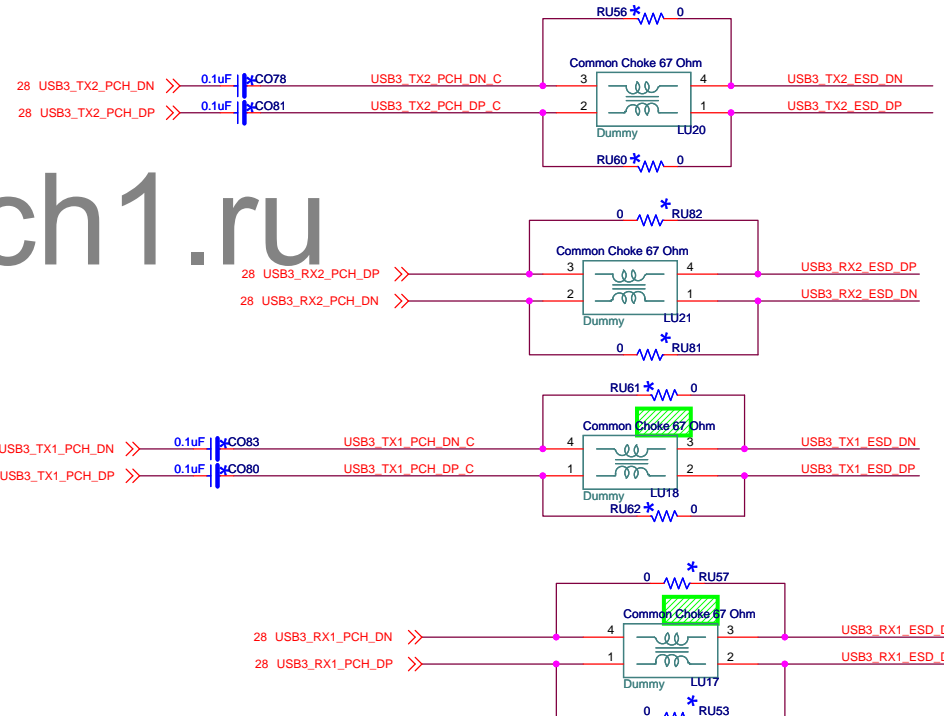
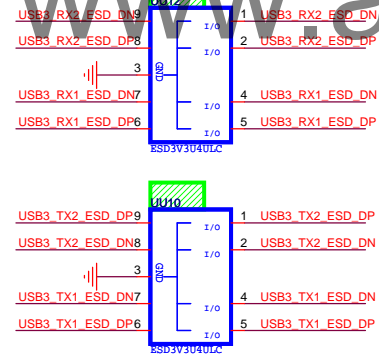
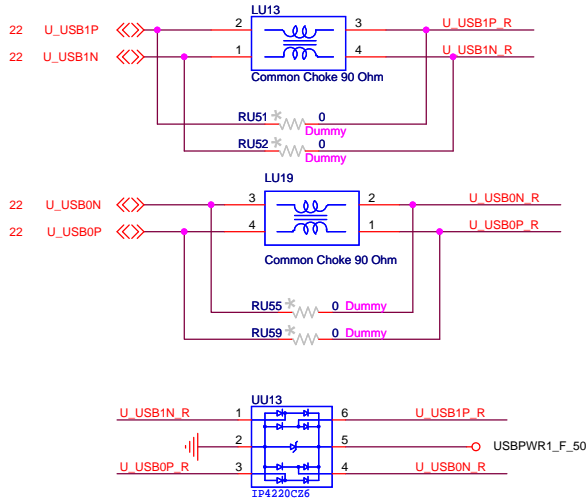
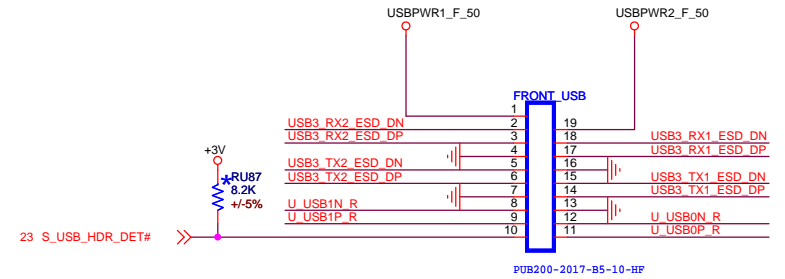
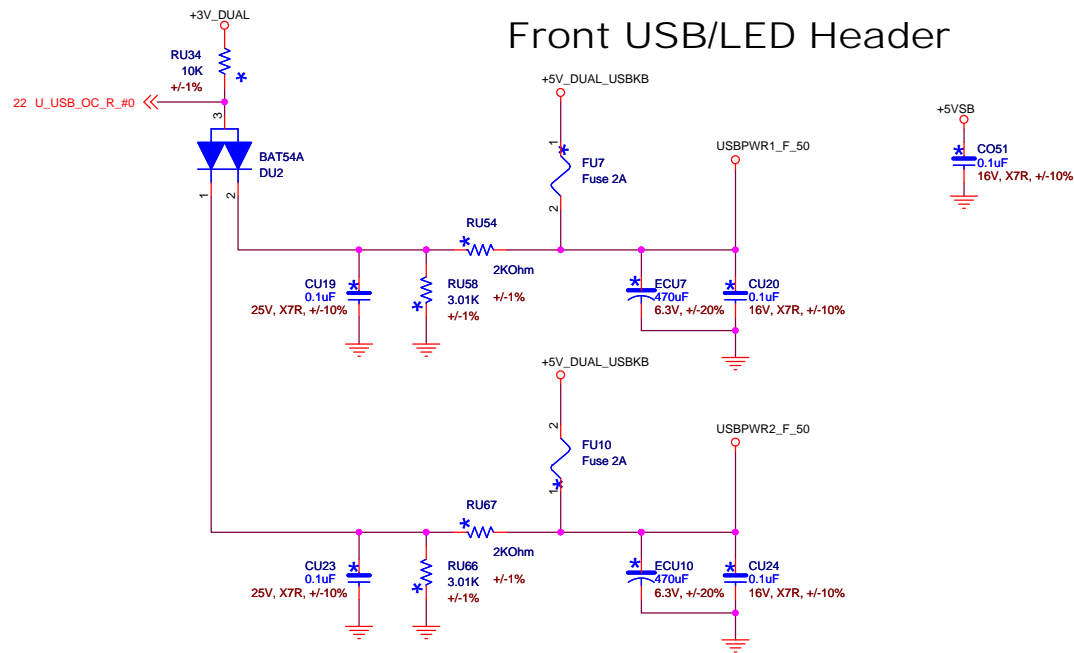
Dummy Serial Port2 header from X01

O_RI2#_R 32



| Title | | |
|--------------------------------|----------|-------|
| COM2 HDR | | |
| DWG NO | Rev | Rev |
| Lanikai_MT/DT | A00 | |
| Date: Wednesday, June 13, 2012 | Sheet 55 | of 71 |

Front USB/LED Header



Transparent top view

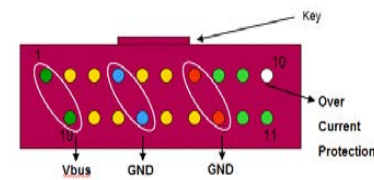


Figure 2-1: USB3 ICC pin numbering



Title

TBD

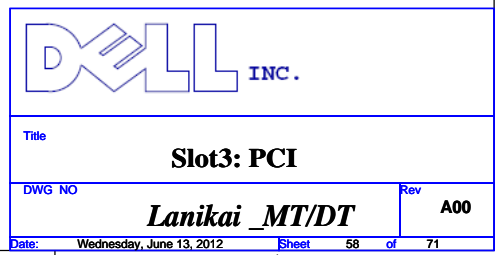
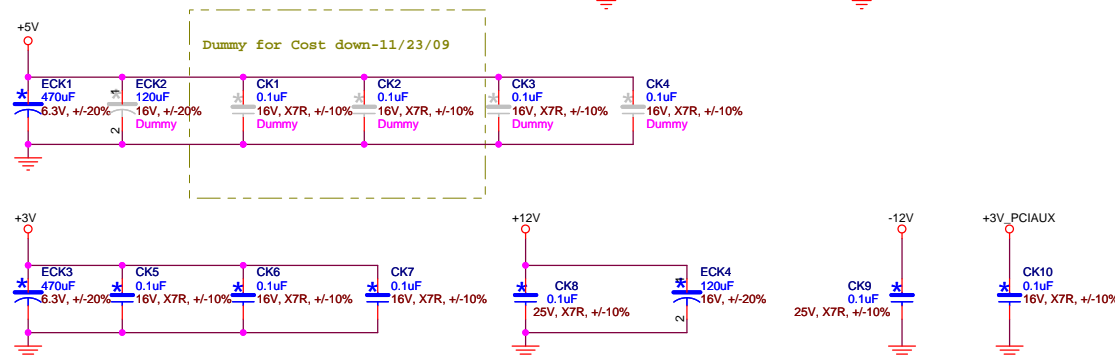
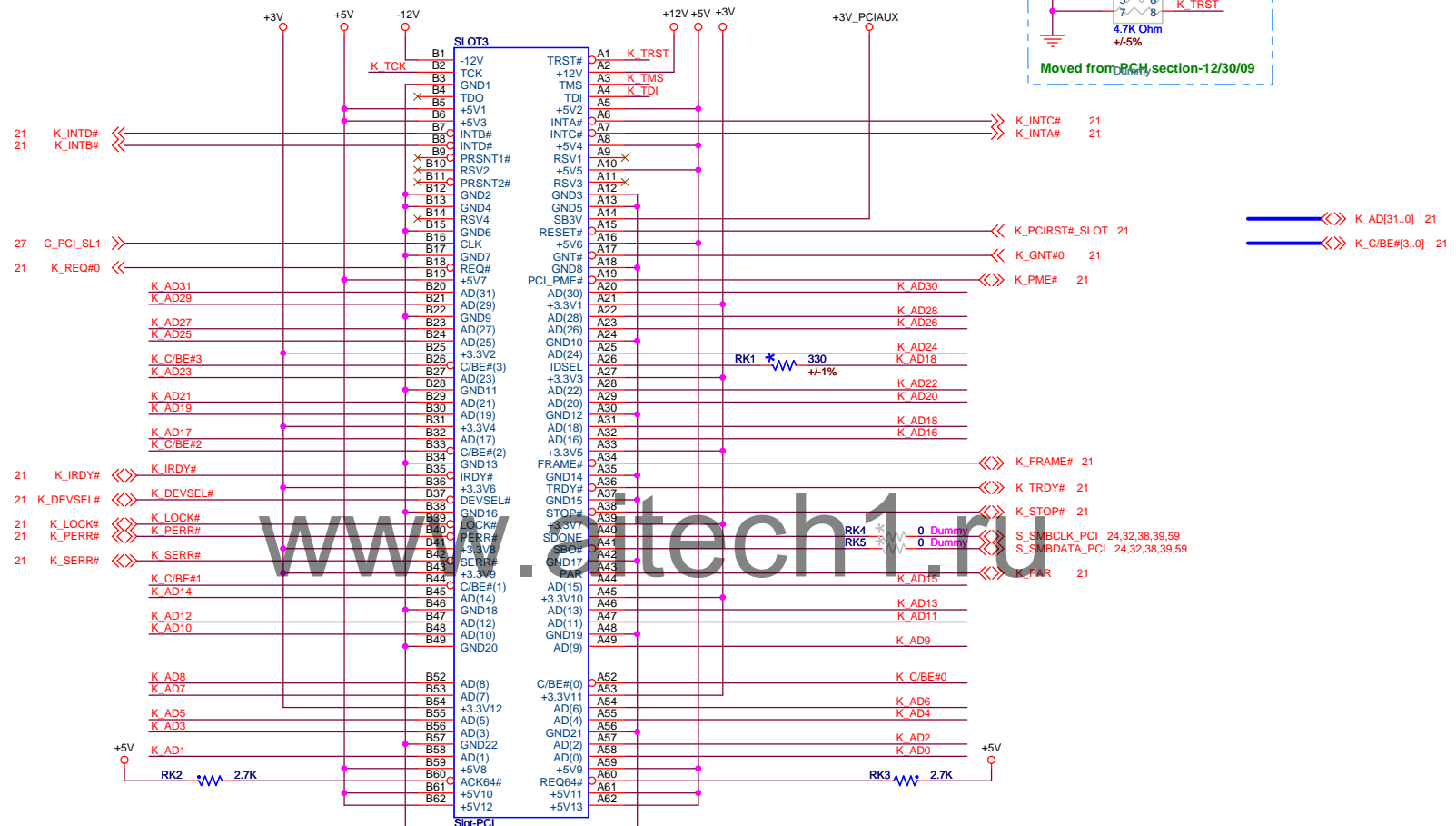
| | |
|--------|--|
| DWG NO | |
|--------|--|

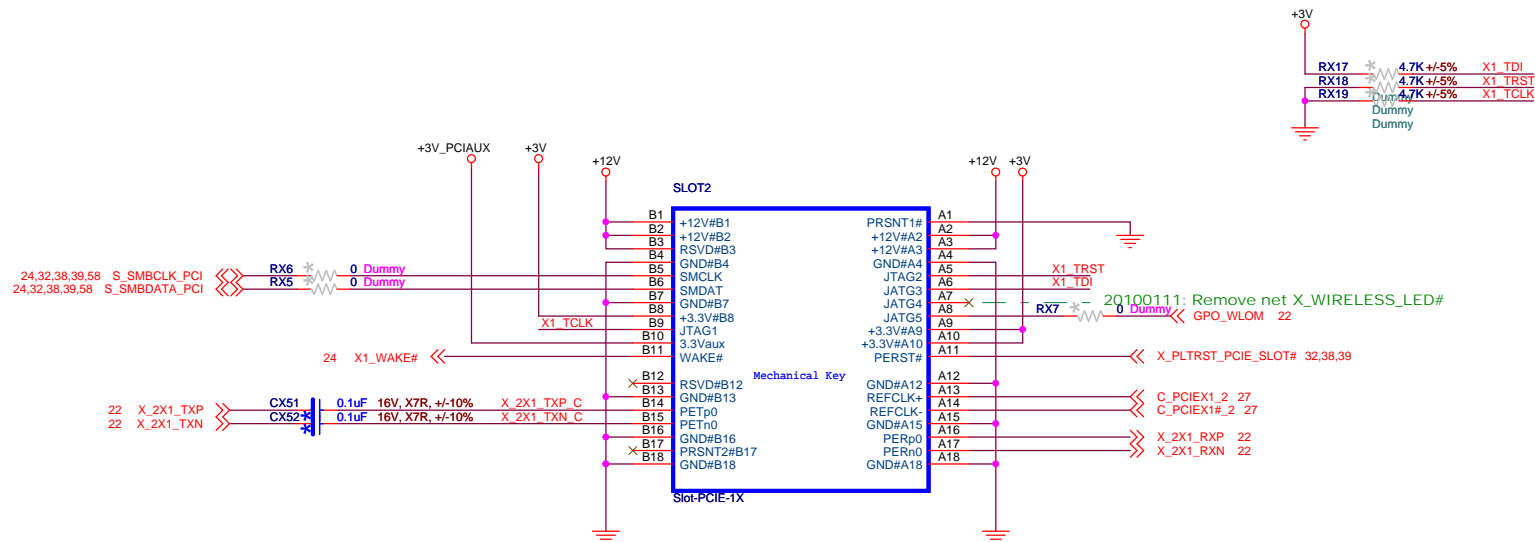
Lanikai MT/DT

Rev

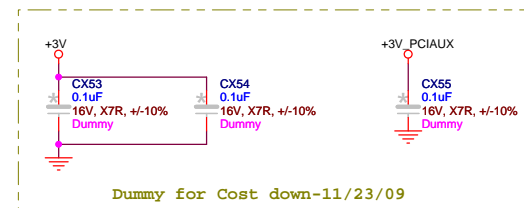
Date: Wednesday, June 13, 2012 Sheet 57 of 71


IRQ: CDAB
IDSEL: AD18
REQ/GNT: 0





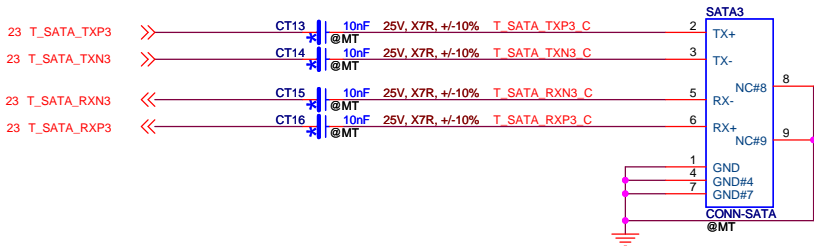
www.aitech1.ru




| | | |
|---|----------------|-----|
|  | | |
| Slot2: PCIe 1x | | |
| Title | DWG NO | Rev |
| Lanikai_MT/DT | A00 | A00 |
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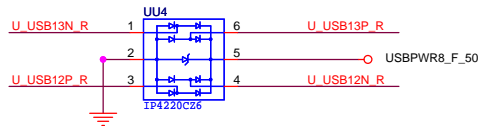
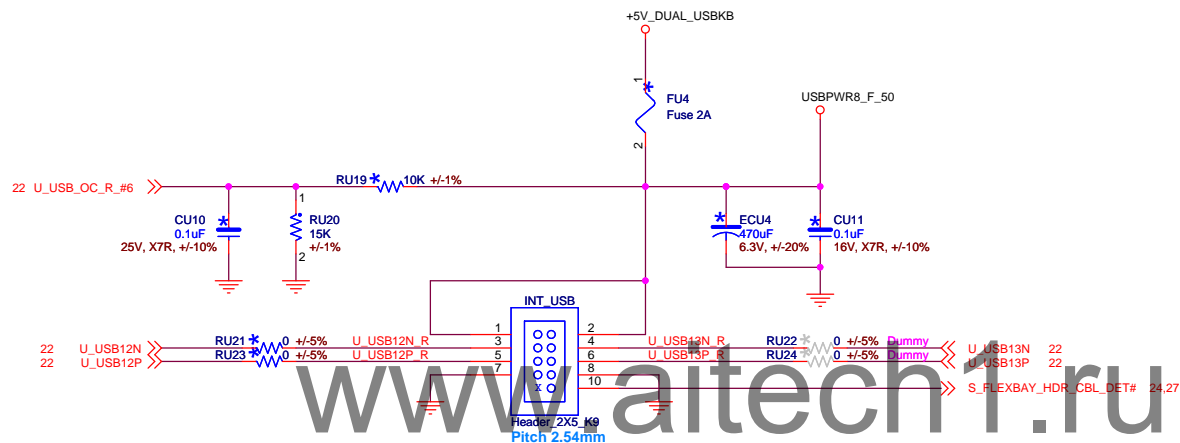
www.aitech1.ru

SATA port 3 only for MT

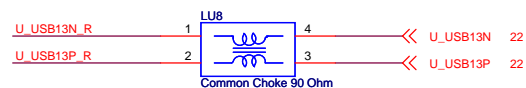
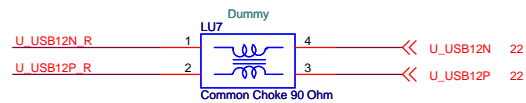


| | | |
|---|--------------------------|----------------|
|  INC. | | |
| Title | | |
| SATA_MT | | |
| DWG NO | | Rev |
| Lanikai_MT/DT | | A00 |
| Date: | Wednesday, June 13, 2012 | Sheet 60 of 71 |

FLEXBAY



stuff on 20100723-EMC request




CO-LAY with 4 Serial resistors RU21, RU22, RU23, & RU24

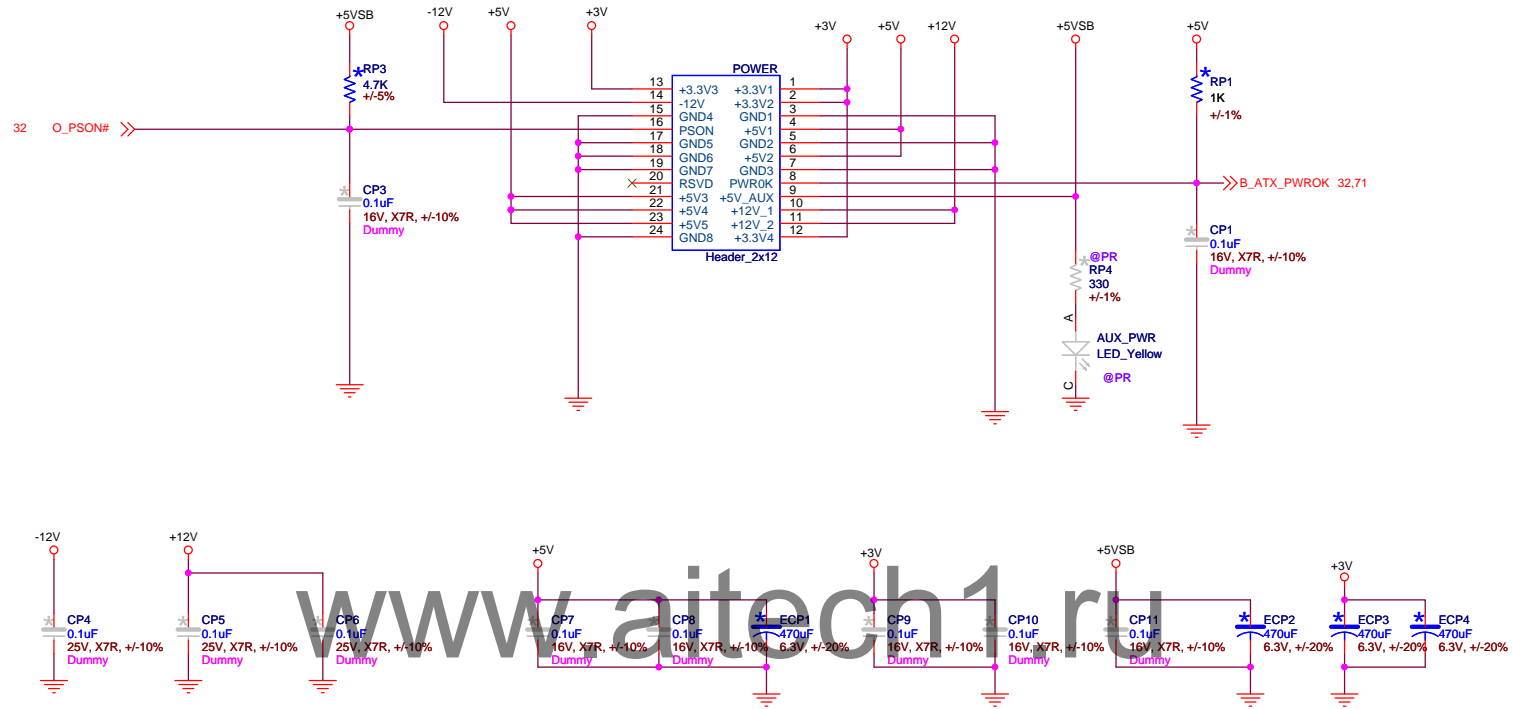
Intel

| | | | | | |
|--------------------------------|--|--|----------------|--|--|
| Title | | | Flexbay USB_MT | | |
| DWG NO | | | Rev | | |
| Date: Wednesday, June 13, 2012 | | | Sheet 61 of 71 | | |
| Lanikai_MT/DT | | | A00 | | |

www.aitech1.ru

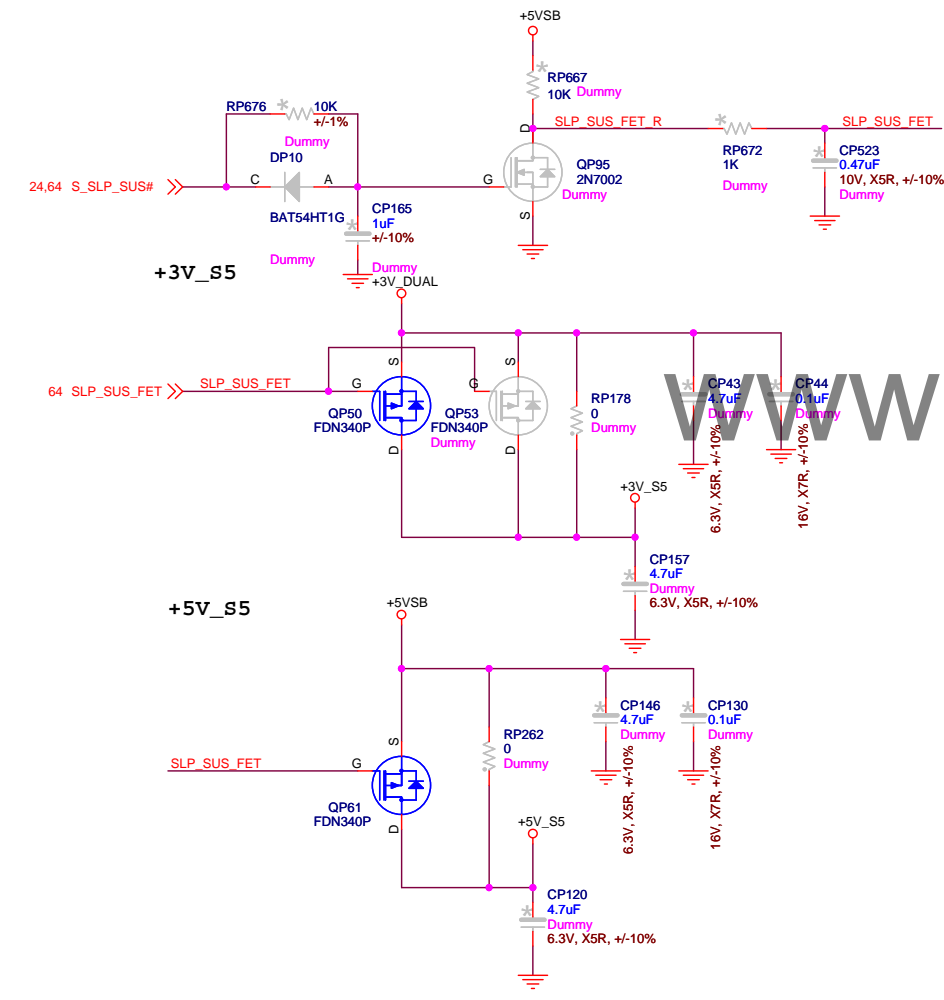
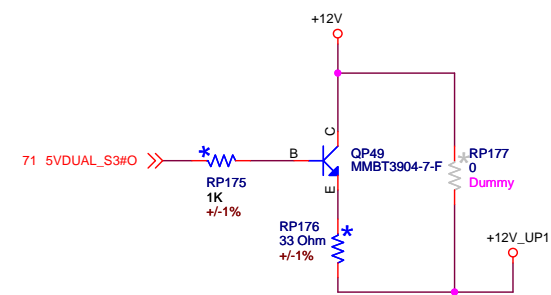
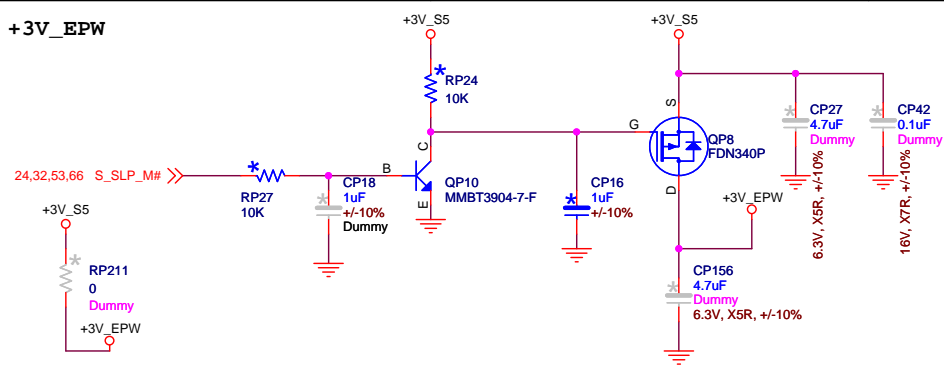
| | |
|---|-------------------|
|  INC. | |
| Title PRT Port | |
| DWG NO Lanikai MT/DT | Rev A00 |
| Date: Wednesday, June 13, 2012 | Sheet 62 of 71 |

ATX POWER CONNECTOR

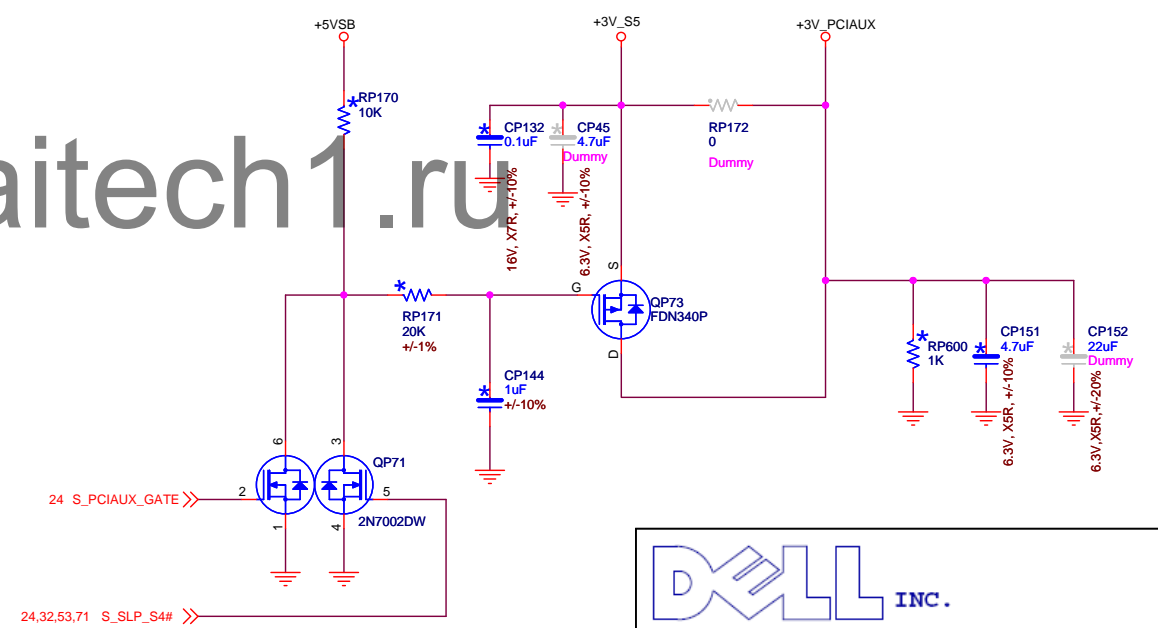


| | | |
|--------------------------------|---------------|---------|
| Title | | |
| Power Conn | | |
| DWG NO | Lanikai_MT/DT | Rev A00 |
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+3V_EPW



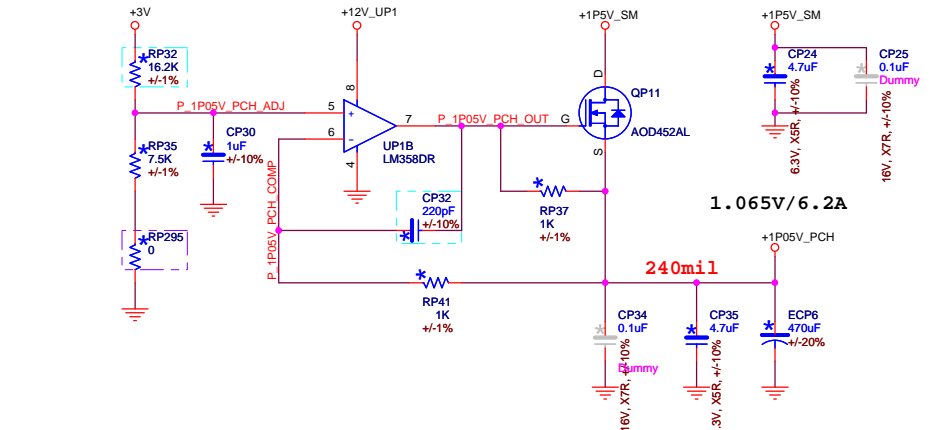
+3V_PCIAUX(FOR PCI/PCIE SLOT)



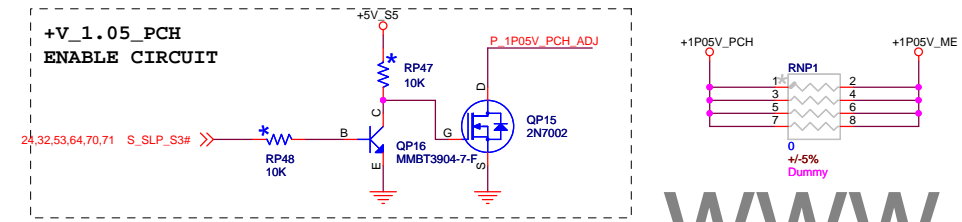
DELL INC.

| | | | |
|--------|--------------------------|-------------------------------|----------|
| Title | | Power-1:Linear Power-1 | |
| DWG NO | | Lanikai_MT/DT | |
| Date: | Wednesday, June 13, 2012 | Sheet | 65 of 71 |

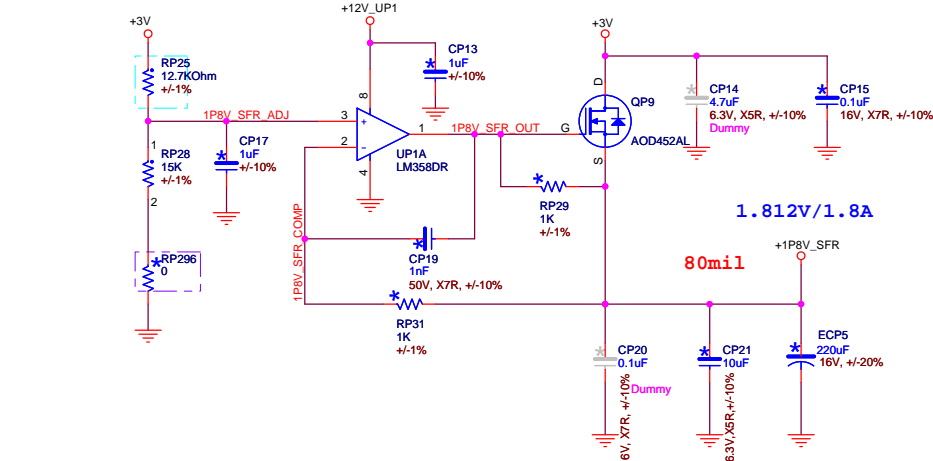
+V_1.05_PCH



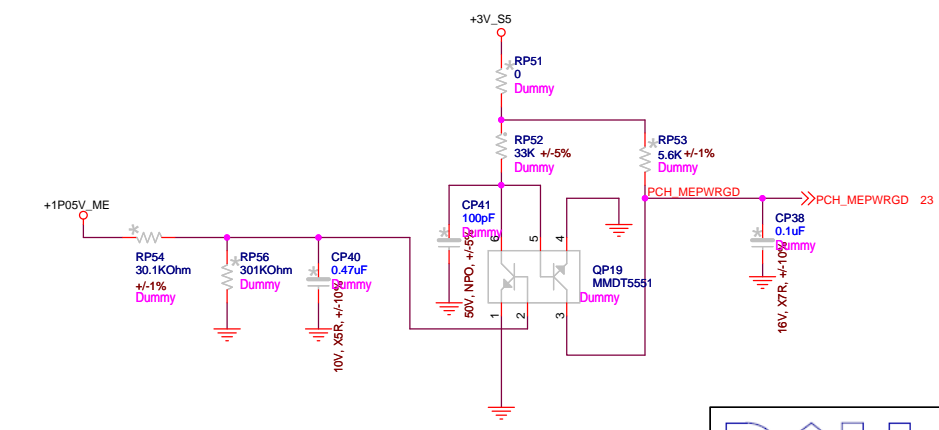
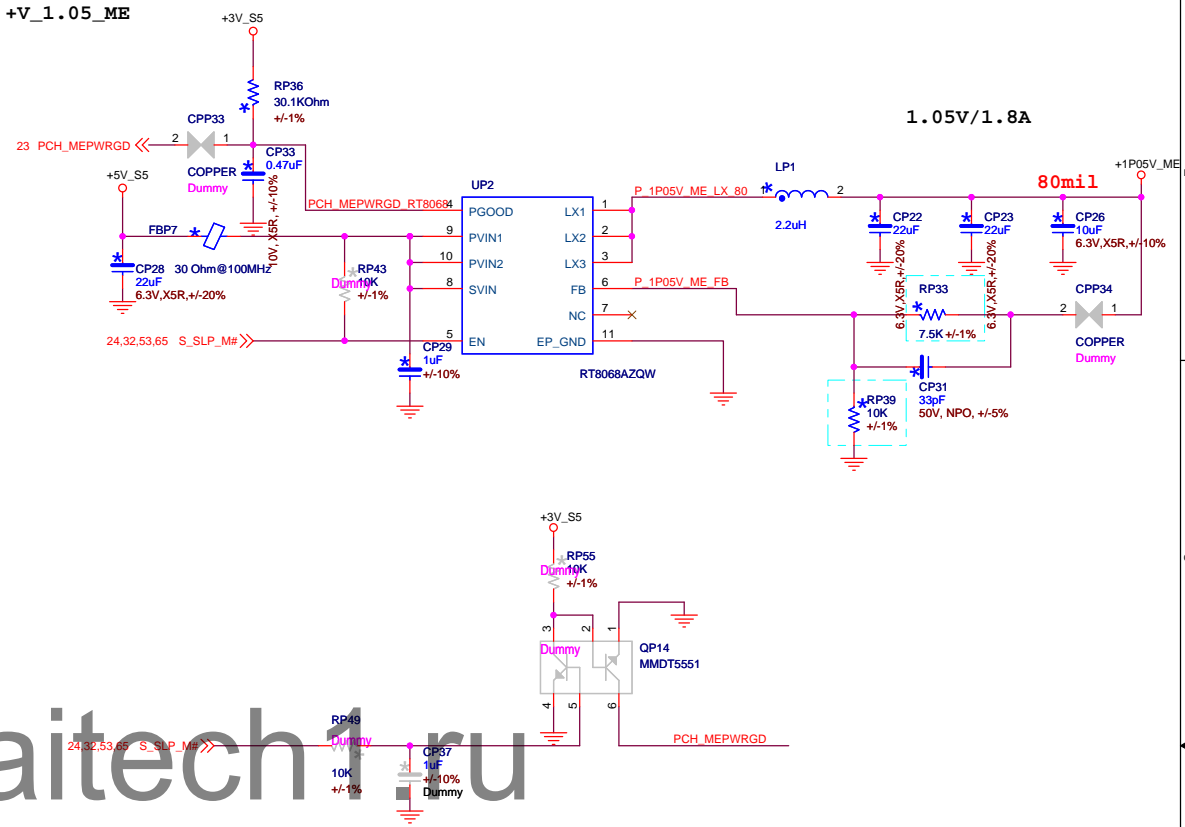
+V_1.05_PCH
ENABLE CIRCUIT



+V_1P8_SFR



+V_1.05_ME



| | | |
|------------------------|--------------------------|----------------|
| Title | | |
| Power-2:Linear Power-2 | | |
| DWG NO | Lanikai_MT/DT | Rev |
| | | A00 |
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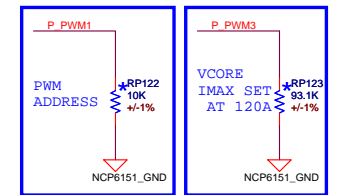
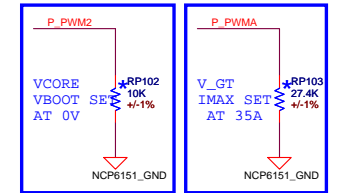
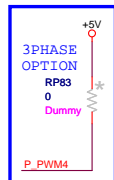
Maho Bay VR12 POWER - 4+1 PHASE

VCC_CORE

VCC_AXG

| PWM ADDRESS | | |
|----------------|-----------------------------|----------------------------|
| RESISTOR VALUE | SVID ADDRESS FOR VCORE RAIL | SVID ADDRESS FOR V_GT RAIL |
| 10K | 0000 | 0001 |
| 25K | 0010 | 0011 |
| 45K | 0100 | 0101 |
| 70K | 0110 | 0111 |
| 95K | 1000 | 1001 |
| 125K | 1010 | 1011 |
| 165K | 1100 | 1101 |

| BOOT VOLTAGE | |
|----------------|--------------|
| RESISTOR VALUE | BOOT VOLTAGE |
| 10K | 0V |
| 25K | 0.9V |
| 45K | 1.0V |
| 70K | 1.1V |
| 95K | 1.2V |
| 135K | 1.35V |
| 165K | 1.5V |



Title

Power-3: Vcore PWM

DWG NO

Lanikai_MT/DT

Date: Wednesday, June 13, 2012

Rev

A00

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